Thesis Defense – Electrical Engineering

Drop Impact Reliability Testing
Lead-Free Chip Scale Packages

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May 23, 2008

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Agenda

- Introduction
  - Drop Impact Reliability
  - Prior Work
  - Thesis Research Goals
- Failure Detection Systems
  - Data Acquisition System Design
  - Post-drop Resistance Measurement
- Test Vehicle Design and Assembly

Agenda

- Drop Impact Testing
- Analysis
  - Reliability Data
  - Failure Mechanisms
  - Acceleration on Test Vehicle
- Conclusions
- Acknowledgements

Drop Impact Reliability

- Mobile electronic devices

  - Are prone to being dropped (or thrown)
  - Are important to our everyday activities
  - Are expected to ‘just work’ even after rough handling

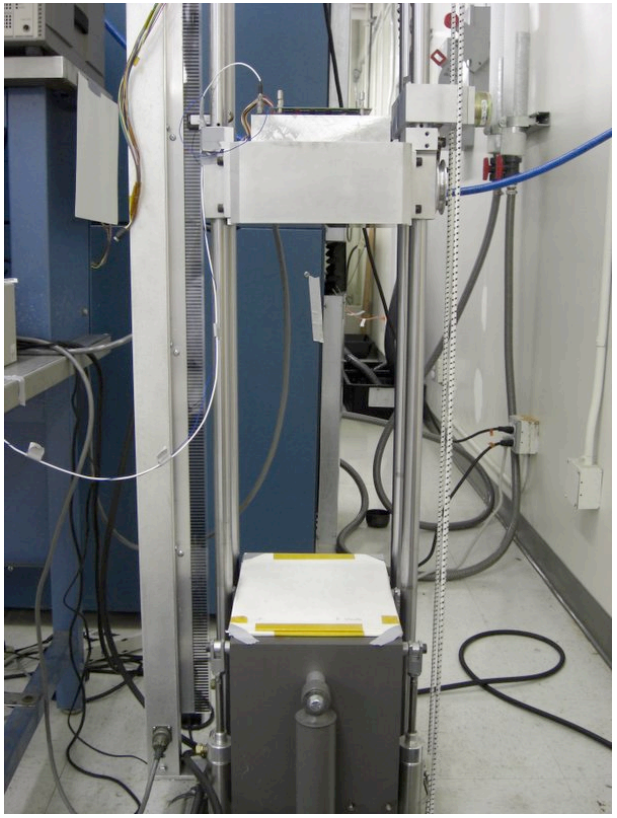
Drop Test Reliability (cont.)

- Mobile electronic devices also…
  - Are complicated and expensive
  - Are easily damaged by drop impacts
  - Are designed to be lightweight and portable
- Drop test reliability is:
  - The study of how well a device or part survives repeated drop impacts
  - A process to determine where design improvements are needed for future high reliability designs

Introduction to Drop Testing

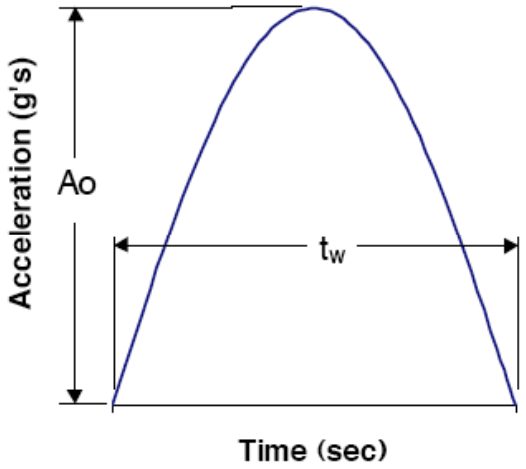
- What happens during a drop impact test
  - The electronics test vehicle is attached to a shock test table
  - The table is dropped vertically until it impacts a stationary base
  - The impact causes an acceleration pulse by rapidly stopping the table (and test vehicle)
  - Test vehicle deforms due to the impact energy, causing stress and strain in the solder joints

Introduction to Drop Testing



Lansmont MTS II Shock Tester

Typical Half-sine Acceleration Pulse



e.g. 1500g - 0.5ms
or 2900g - 0.3ms

Drop Impact Reliability

- Drop impact reliability testing evaluates the reliability of electronics when subjected to mechanical shock
  - Shock causes vibration, PWB bending, and resulting mechanical stresses on solder joints
- Generally focused on lead-free solder usage in consumer electronics (handheld products)
  - Due to governmental regulations pushing toward a world-wide lead-free market for these products

Introduction to Drop Testing

- The drop impact test
  - Is repeated until failure occurs
  - Determines how many drop impacts of a specific intensity (acceleration peak and duration) can be survived before the device fails
- Drop impact reliability data is a tool that can guide designers in developing more robust electronic products

Drop Impact Demo

Why Study Lead-free Solder?

- Environmental regulations and directives currently restrict the use of lead in consumer electronics products within global markets
  - European Union's Restriction of Hazardous Substances (RoHS)
  - China's Regulation for Pollution Control of Electronics Products (RPCEP)
  - And more…

Why Study Lead-free Solder?

- Lead-free solder is still very new to the electronics industry
  - RoHS regulations took effect in 2006
- Many lead-free solder alloys can be used to replace tin-lead solder, and more information is needed on their performance

Prior Work

- Researchers have studied
  - Lead-free SnAgCu solder alloys and various micro-additives in the alloys to improve reliability
  - Use of underfill and Corner Bonding to improve mechanical strength and reliability of components
  - Board and device level drop impact reliability, acceleration, stress, and strain on solder joints for many component and solder joint sizes

Purpose of this Thesis

- Develop a high-speed data acquisition (DAQ) system for drop impact reliability research
- Determine the drop impact reliability of lead-free Chip Scale Package (CSP) solder joints

Purpose of this Thesis

- Determine the effects of edge bonding on CSP drop impact performance
- Investigate the failure mechanisms of drop impact failures in lead-free CSPs

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Drop Impact Failure Detection

- Goal: Develop a high-speed DAQ failure detection system for drop impact reliability research
- System should:
  - Detect intermittent failures by testing resistance during the drop impact (in-situ testing)
  - Save all sampled data for later analysis
  - Require minimal operator interaction so that highly repetitious testing can be done without interruption

Definition: Drop Impact Failure

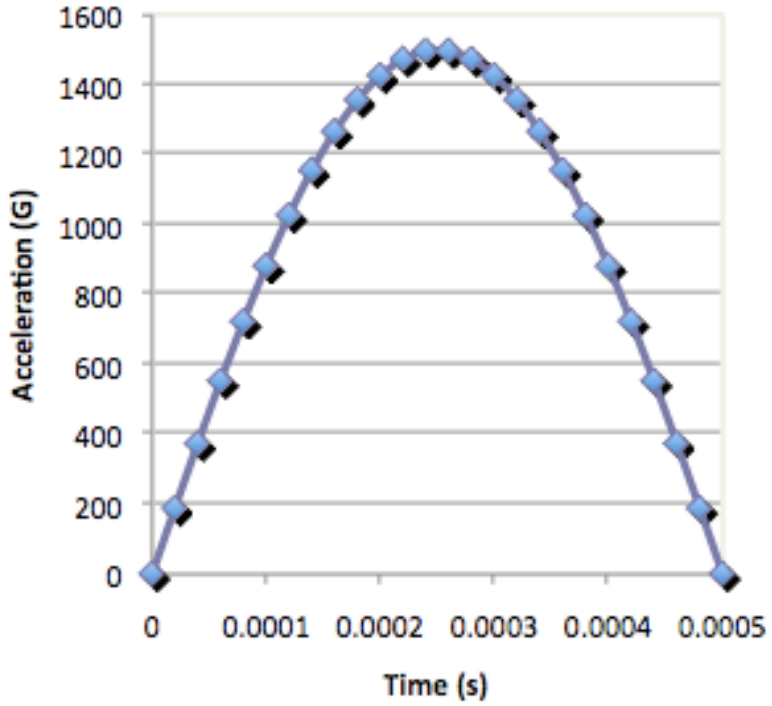
- Drop impact failure…
  - Occurs when the electrical connections in the device are damaged so that it no longer functions as designed
  - Is typically detected by change in resistance or loss of continuity in board level circuits
  - May be either a permanent or intermittent condition

Drop Impact Failure Detection

- Joint Electron Device Engineering Council (JEDEC) recommendations
  - Specified in the JESD22-B111 standard for handheld electronics drop impact testing
  - Identify failure as 100 ohm change in resistance
  - Sample resistance at a minimum frequency of 50kHz to observe intermittent failures
    - A rate much higher than the vibration frequencies of the test vehicle after impact so that accurate reproduction of the resistance change is observed (no aliasing)

Drop Impact Failure Detection

- Visualization of a sampling frequency of 50Khz during a typical drop impact
  - 50000 samples per second, 25 samples per 0.5ms



Representation of a 1500g – 0.5ms acceleration pulse sampled at 50kHz

Data Acquisition System Design

- System composed of:
  - Multichannel voltage divider resistance measurement circuit
  - National Instruments analog-to-digital converter (ADC) PCI card
  - Desktop computer
  - ADC control and data gathering software
  - Cable from test vehicle to connector boxes
  - External trigger

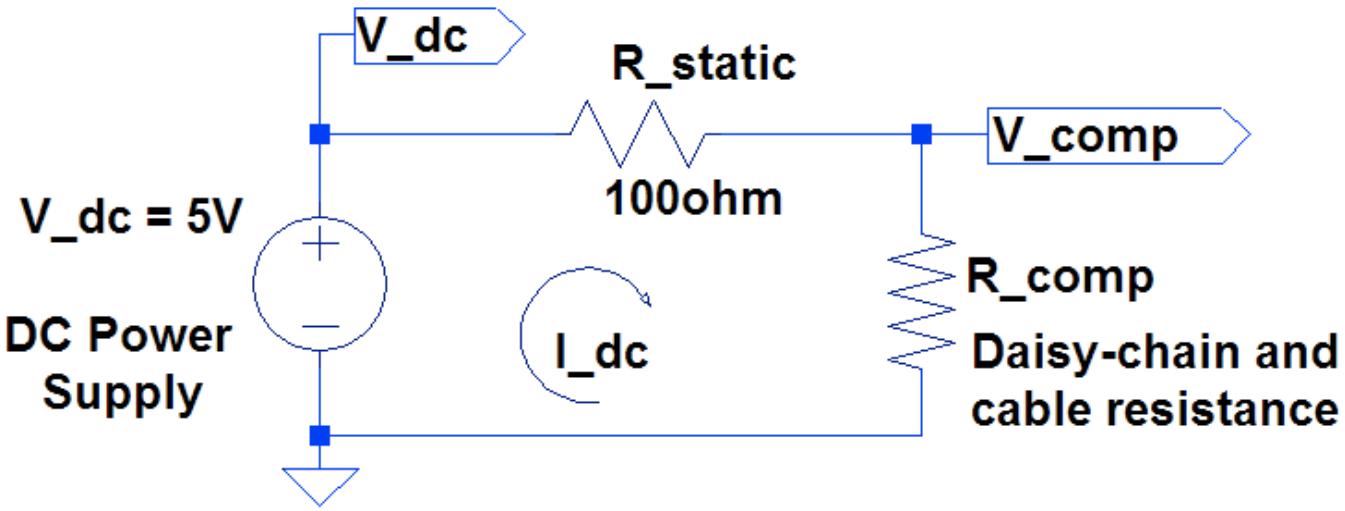
Voltage Divider Circuit

- Dynamic resistance measurement is achieved by using a series voltage divider circuit to relate voltage to resistance
  - The ADC measures voltage divided between the static resistor and component resistance

$$V_{Comp} = V_{DC} \cdot \frac{R_{Comp}}{R_{Comp} + R_{Static}}$$

$$R_{Comp} = \frac{V_{Comp} \cdot R_{Static}}{V_{DC} - V_{Comp}}$$

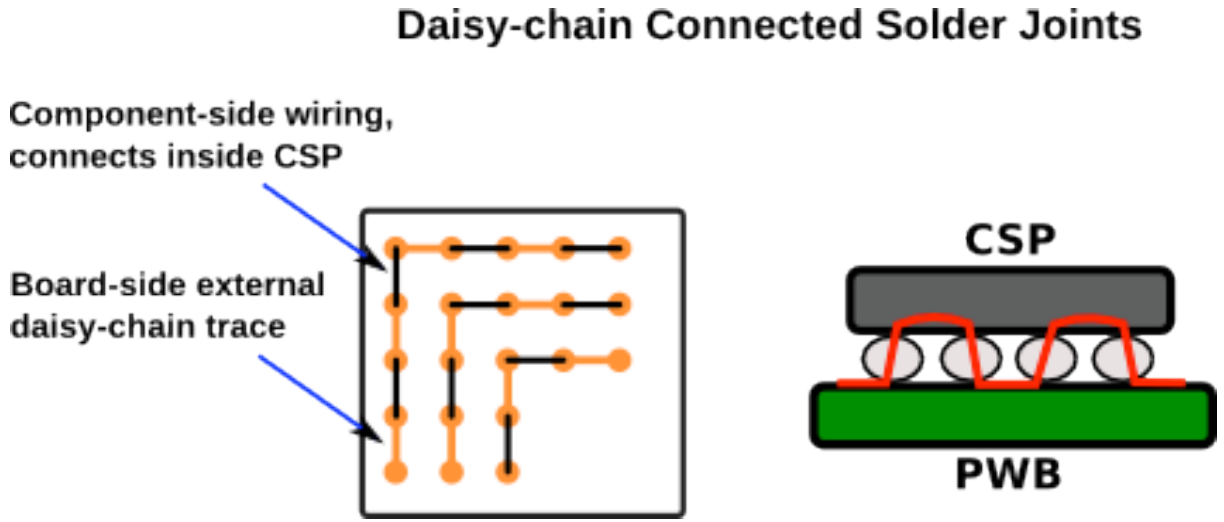
Voltage Divider Circuit



$$R_{Comp} = \frac{V_{Comp} \cdot R_{Static}}{V_{DC} - V_{Comp}}$$

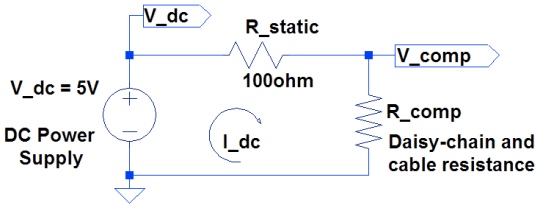
Voltage Divider Circuit

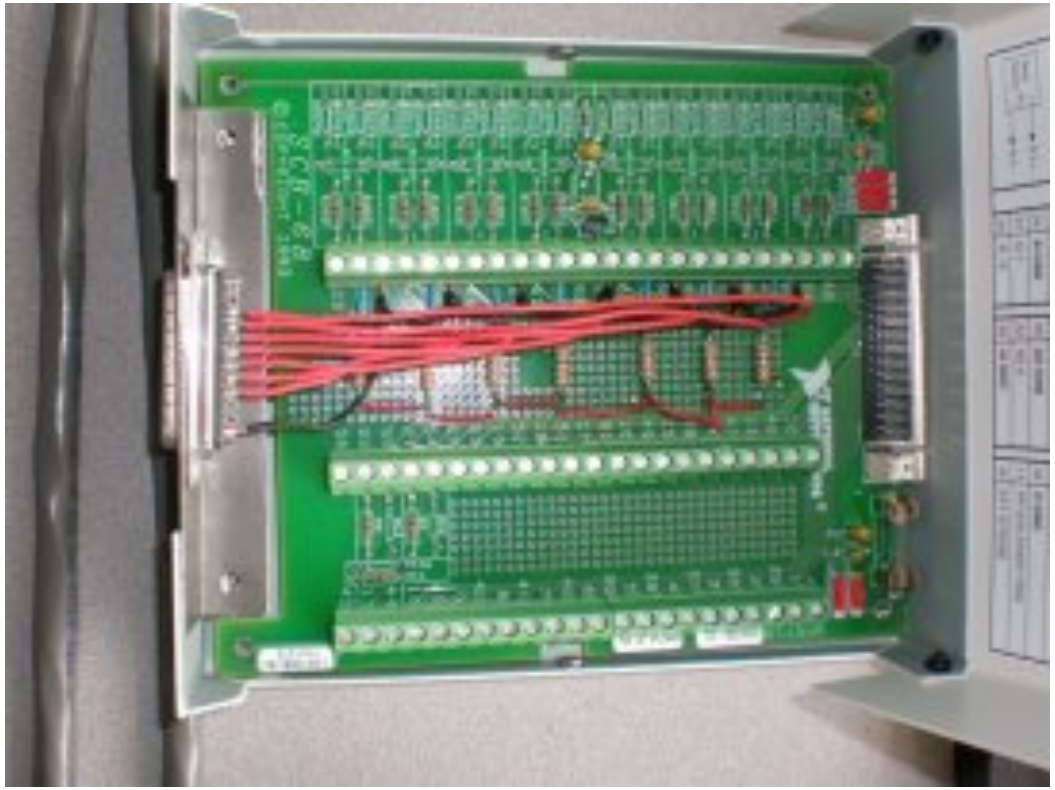
- The component solder joints are connected together into a daisy-chain, forming a single ‘wire’ connecting many tiny resistors (solder joints) and circuit board traces



Voltage Divider and Connector Boxes

- The voltage divider circuit is assembled within two National Instruments connector boxes





Voltage Divider and Connector Boxes

- DAQ parallel cable connections were added to the front of these boxes

Connector Box front

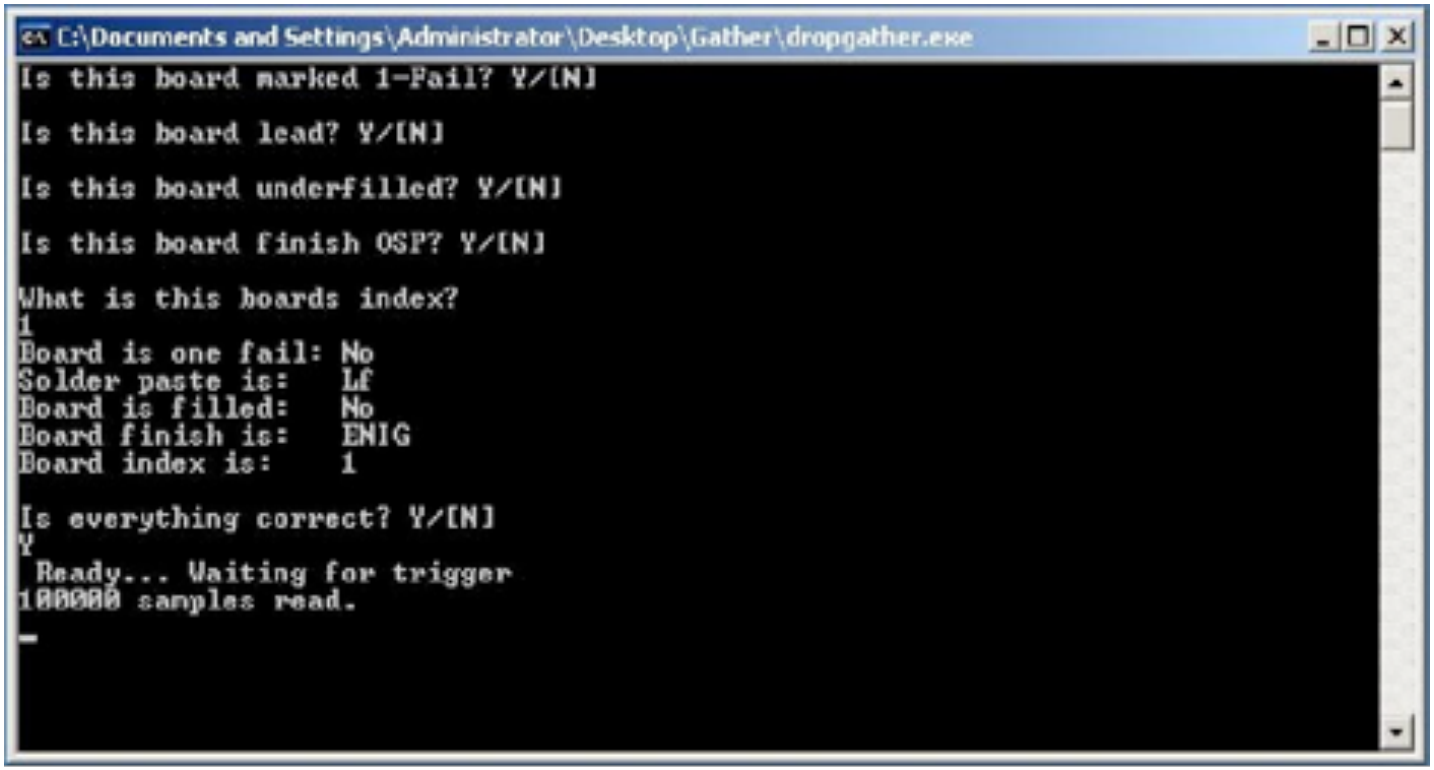
Cable attached to Connector Boxes

DAQ System – Software

- DropGather
  - Windows console-based program written in C++
  - Interfaces to National Instruments DAQmx driver libraries for ADC device control
  - Released as open source software for others to use as an example in building similar systems

DAQ System – Software

- DropGather
  - Windows console-based program written in C++

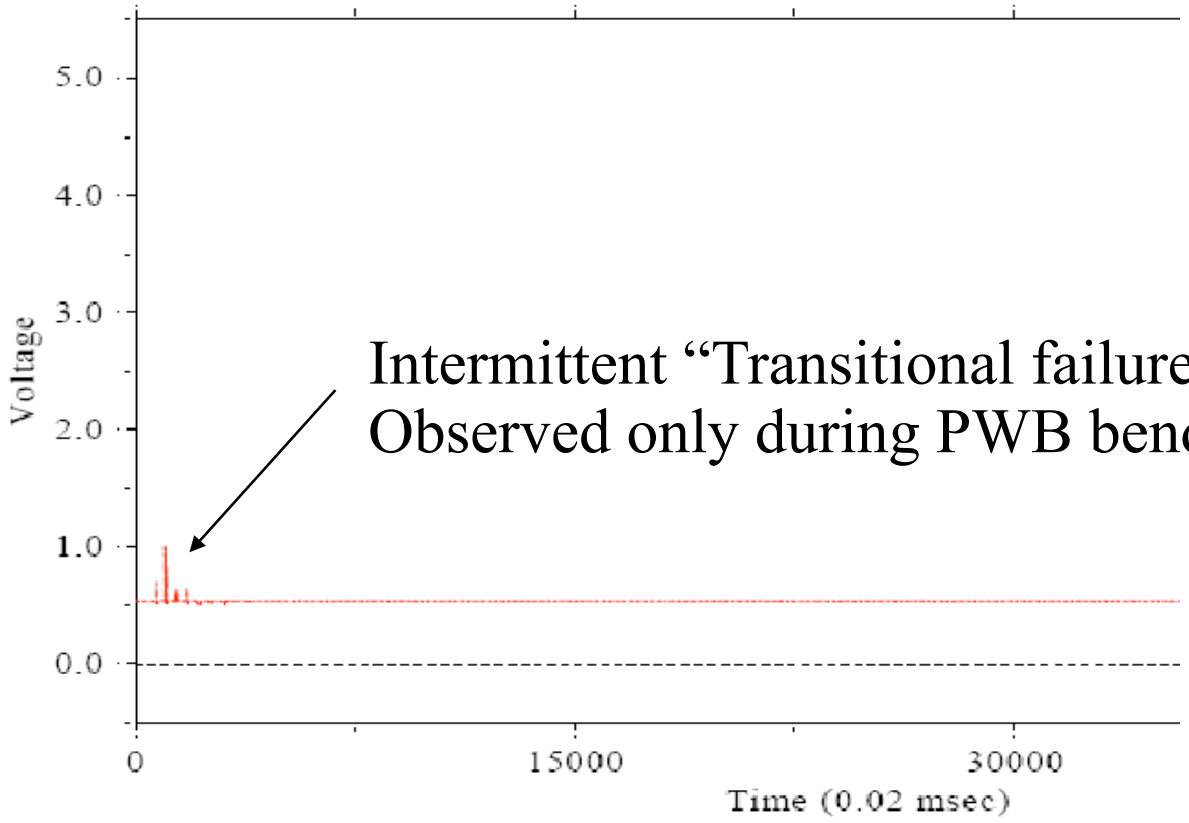


Data Acquisition System Summary

- DAQ system capabilities
  - 17 channels (15 for components, power supply voltage, trigger)
  - Sampling frequency of 50kHz per channel
  - 16 bit measurement accuracy (over 0-5V range)
  - Store entire data set for later analysis
    - Tab-separated-text (CSV) data value tables
    - PDF format graphs of each measured channel

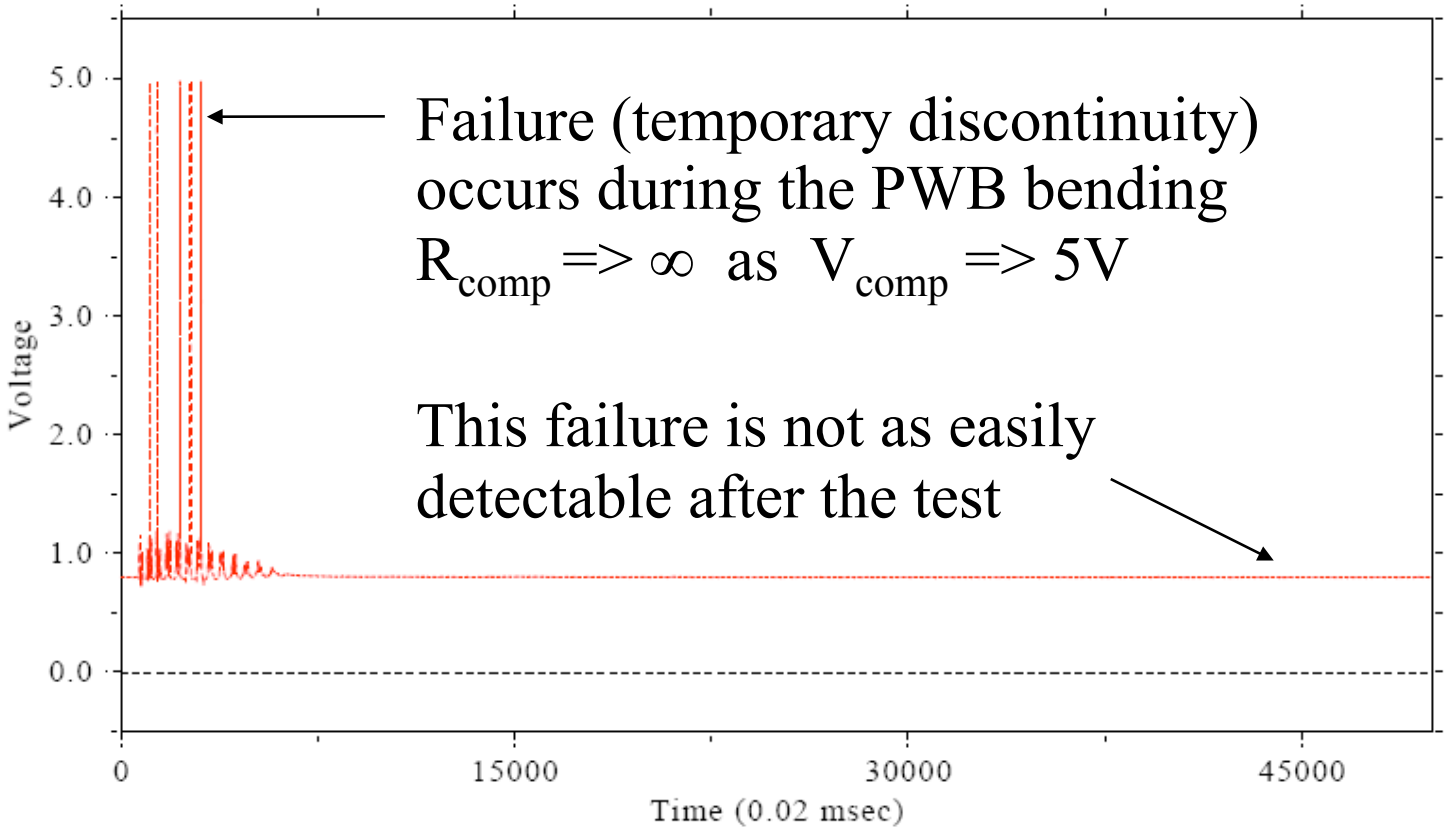
Failure Event Graphs

- Display results plot: time vs sampled voltage



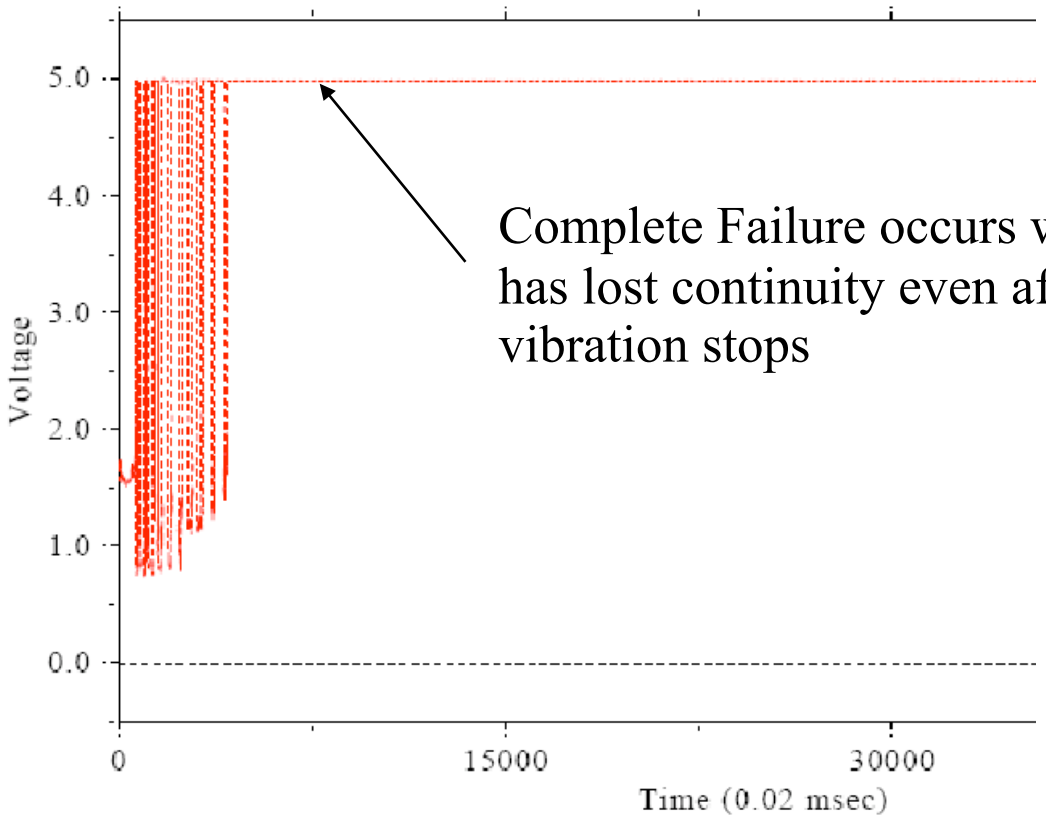
Failure Event Graphs

- Display results plot: time vs sampled voltage



Failure Event Graphs

- Display results plot: time vs sampled voltage



Complete Failure occurs when the daisy-chain has lost continuity even after the PWB vibration stops

Failure Detection Systems

- Compare two failure detection systems
  - High-speed DAQ dynamic resistance measurement
  - Post-drop static resistance measurement
    - Commonly used in industry

Post-Drop Testing

- Uses a single resistance measurement per drop taken after the board vibration ceases
- Failure when a 10 ohm static rise is detected
- Monitor resistance change over multiple drop period
- LabView program which configures Keithley equipment to collect resistance values
- Outputs tabular data for resistance of all 15 components once each drop

Post-Drop Testing

- Advantage:
  - No wires soldered to the test board, fast setup
  - Low cost system
- Disadvantages:
  - Cannot test in-situ (during board deflection and vibration conditions)
  - Requires operator interaction every drop cycle
  - Only one test per drop provides fairly poor resolution for when failure occurs

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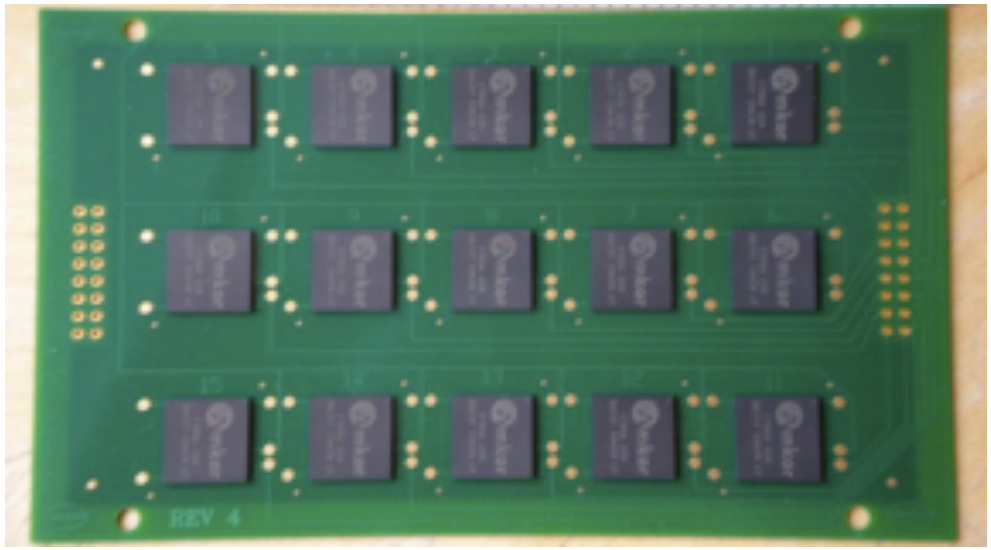
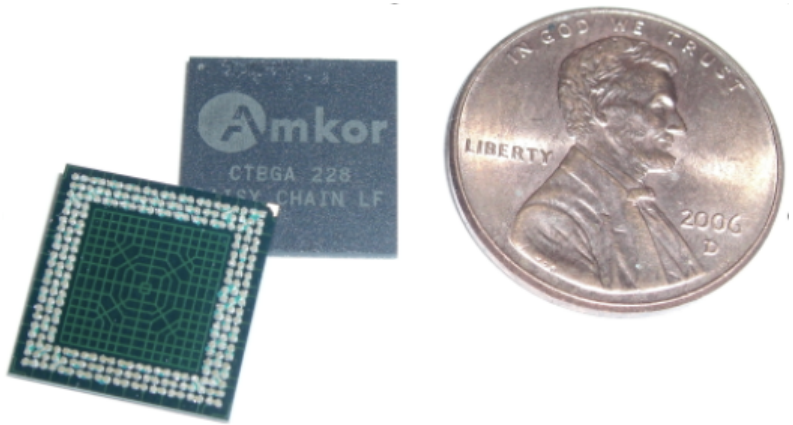
Test Vehicle Design

- JEDEC JESD22-B111 preferred board
  - 8-layer FR4
  - 132 mm x 77 mm in size (roughly 5.2” x 3.0”)
  - 15 components in a 3 row by 5 column array



SMT Assembly (cont.)

- Components (Amkor)
  - Amkor CSPs A-CTBGA228-.5mm-12mm-DC-LF
  - 12 mm x 12 mm
  - 228 I/Os (perimeter array, daisy-chain connected)
  - 0.5mm pitch

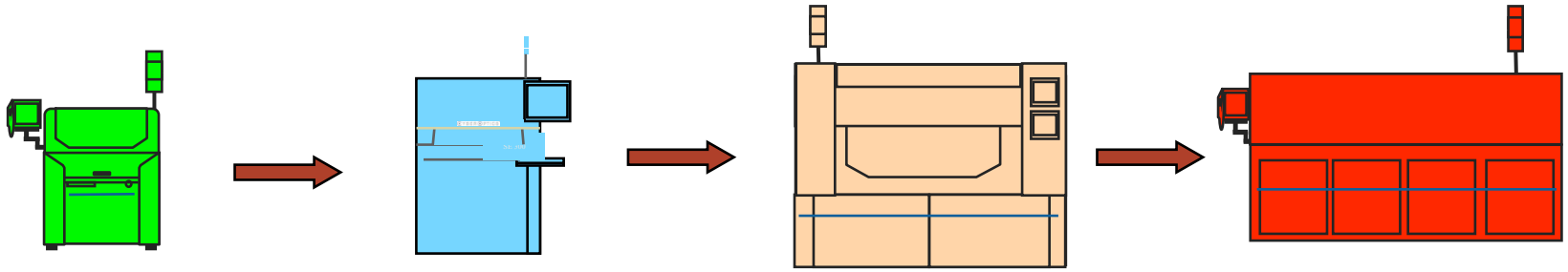


SMT Assembly (cont.)

- Lead-free Solder Paste
  - Multicore 318 LF 97SC
  - $SnAg_{3.0}Cu_{0.5}$ alloy composition (also called SAC305)
  - Primarily tin with 3.0% silver and 0.5% copper by weight
  - Common replacement for tin-lead solder

SMT Assembly

- Dedicated lead-free SMT assembly line



DEK Stencil Printing

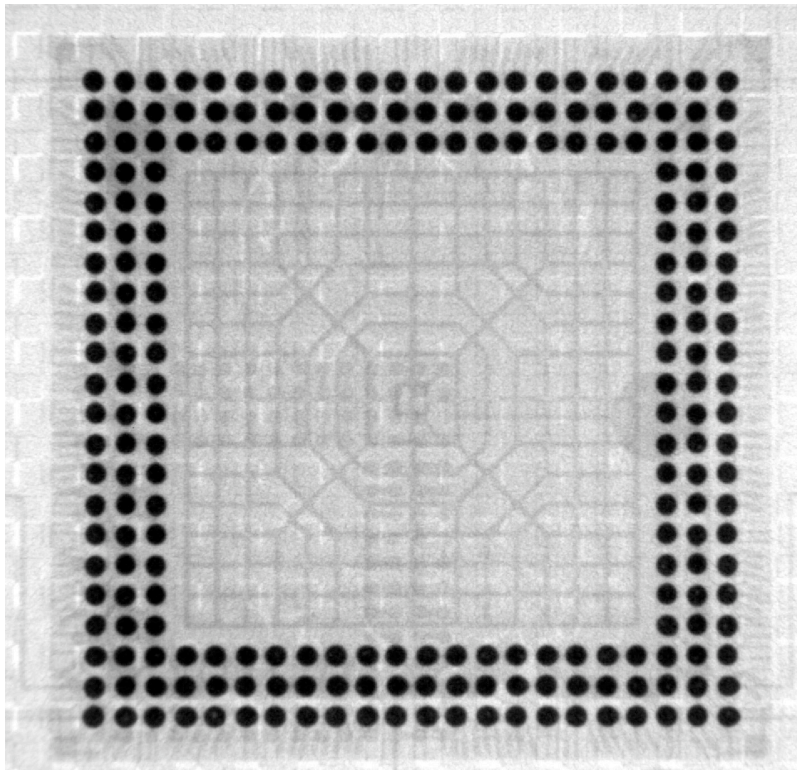
CyberOptic Solder Paste Inspection

Siemens F5 Placement

Heller Oven EXL1800

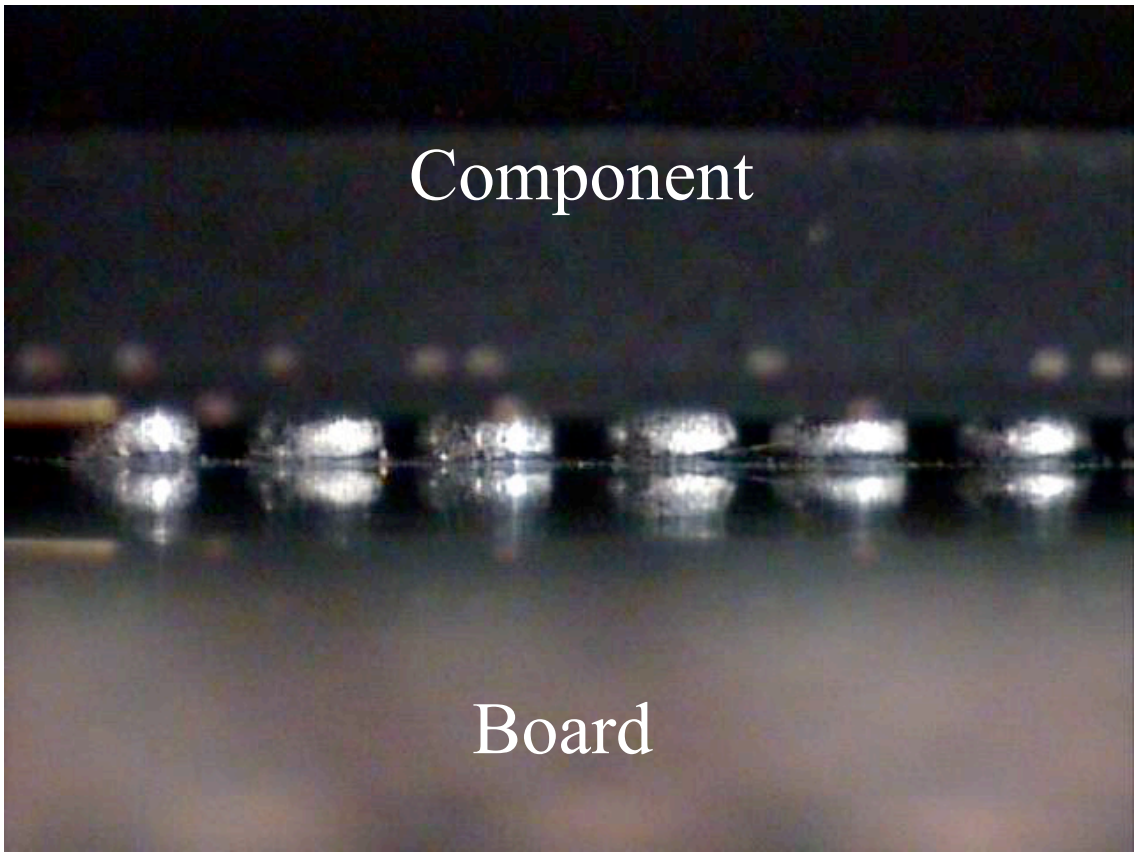
Solder Joint Integrity after Assembly

- The X-Ray image shows solder balls are round and uniform, no visible bridging is present



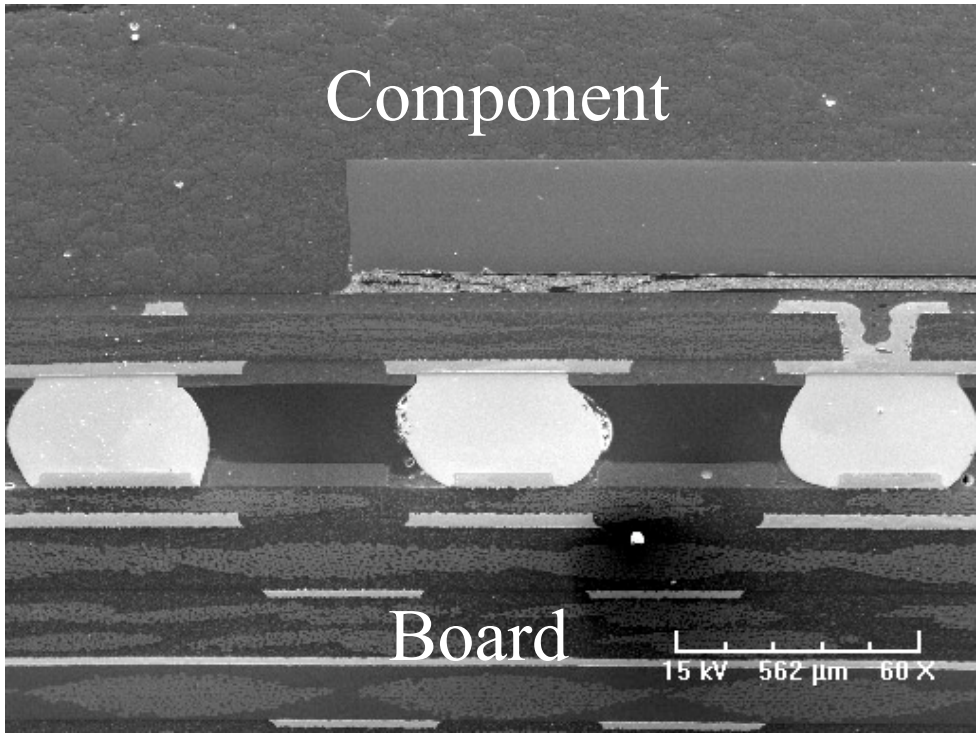
Solder Joint Integrity (Cont.)

- The solder balls look shiny and well collapsed



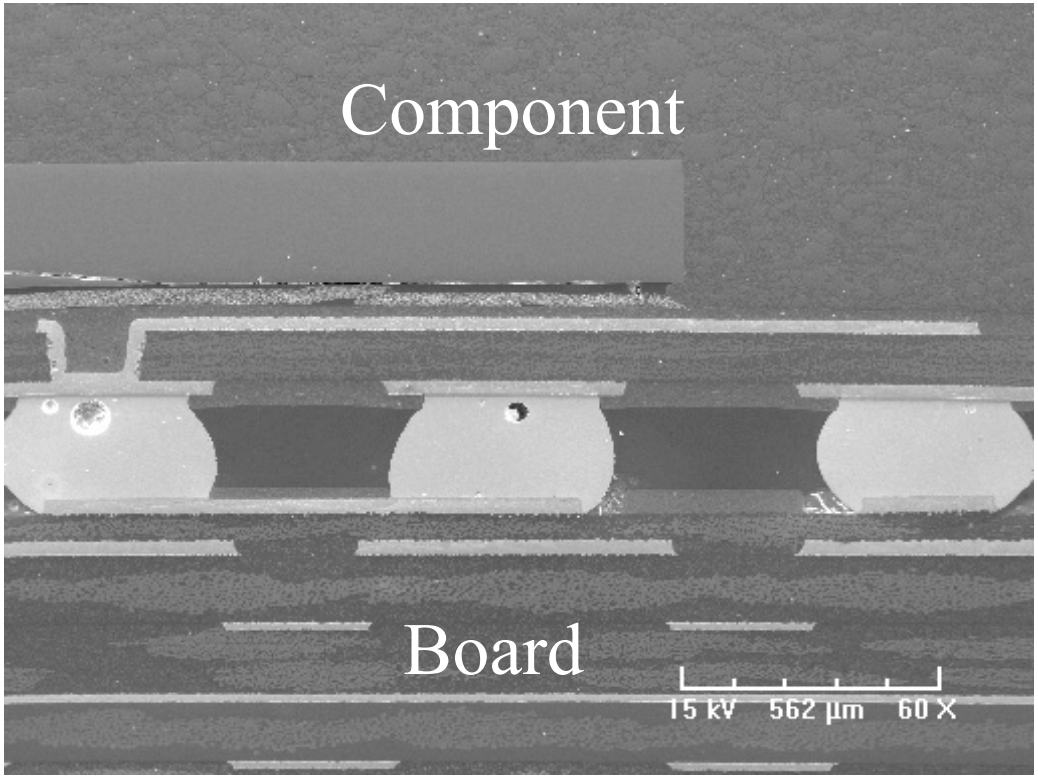
Solder Joint Integrity (Cont.)

- SEM image of cross-sectioned CSP shows good solder joints



Solder Joint Integrity (Cont.)

- SEM image of cross-sectioned CSP shows some voids



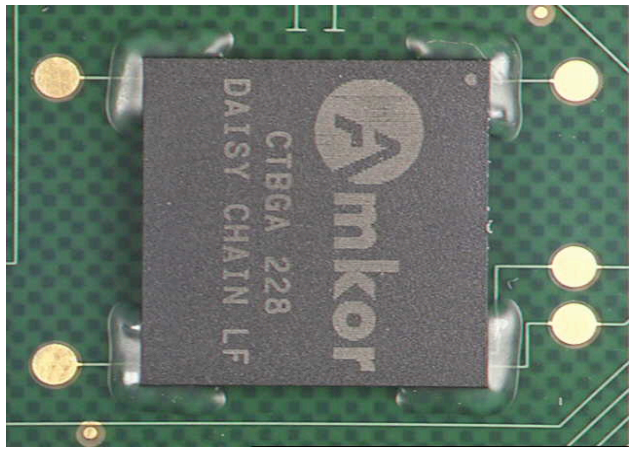
Edge Bonding for Strength

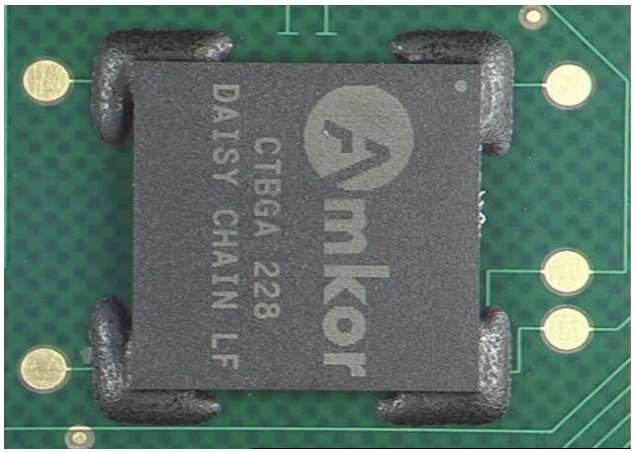
- Edge Bonding is a process that applies a glue material to the corners of components
  - Intended to increase mechanical strength of the component to board connection
  - Relieves some stress on the solder joints
  - Similar glues are used for full capillary underfill and Corner Bonding

Edge Bond Materials

- Edge bond application for 12mm CSPs
  - Acrylated Urethane-based material
    - Cured by UV exposure for 80s using Zeta 7411 Lamp
  - Epoxy-based material
    - Thermally cured for 20min in 80° C oven

Acrylic





Epoxy

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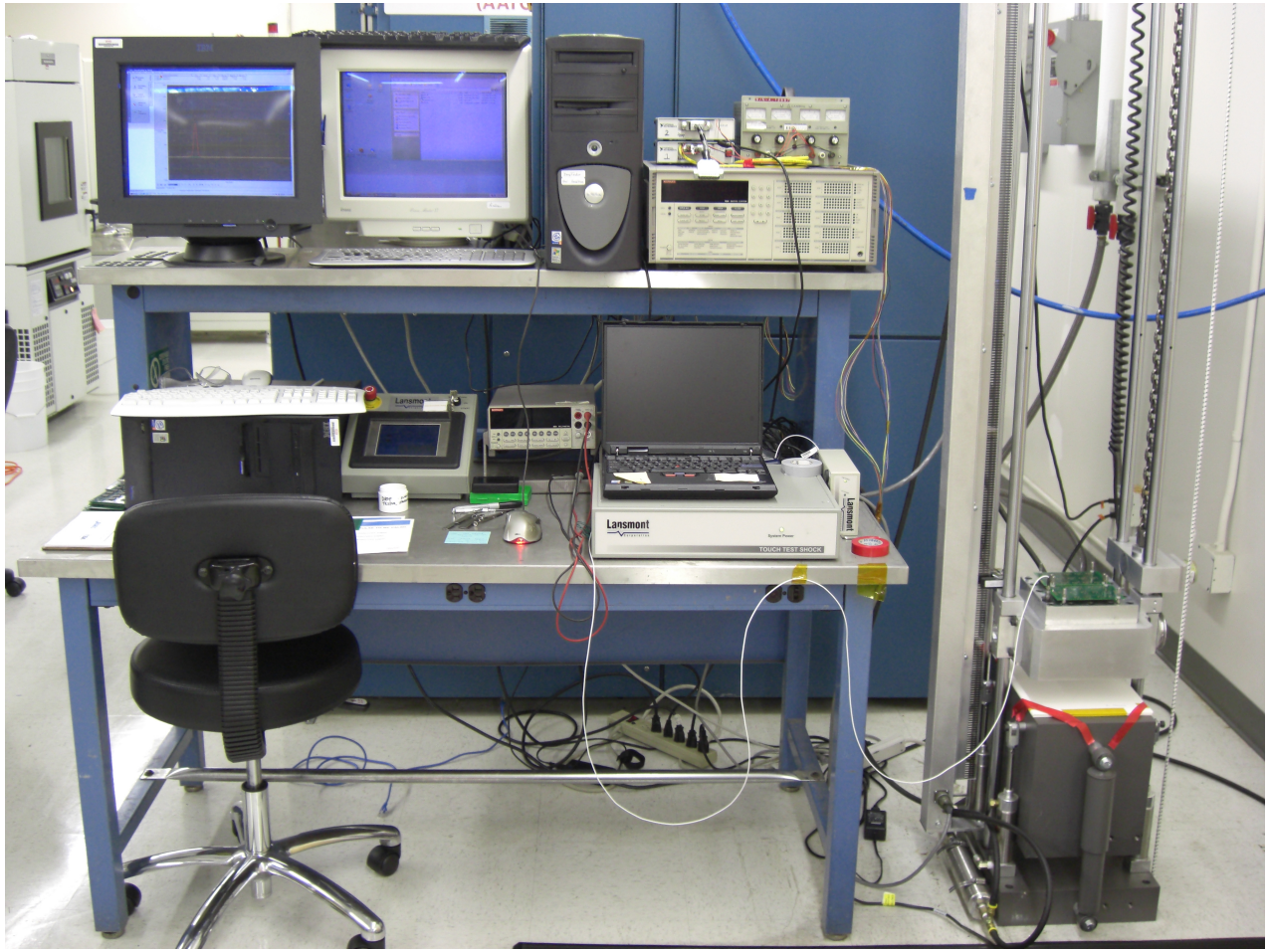
Reliability Test Design

- Drop tests were conducted at Henkel Electronics in Irvine, CA, during Summer ‘07 internship
  - This is a Henkel Corporation R&D facility focused on adhesives, packaging, and bonding agents

Drop Testing Workbench

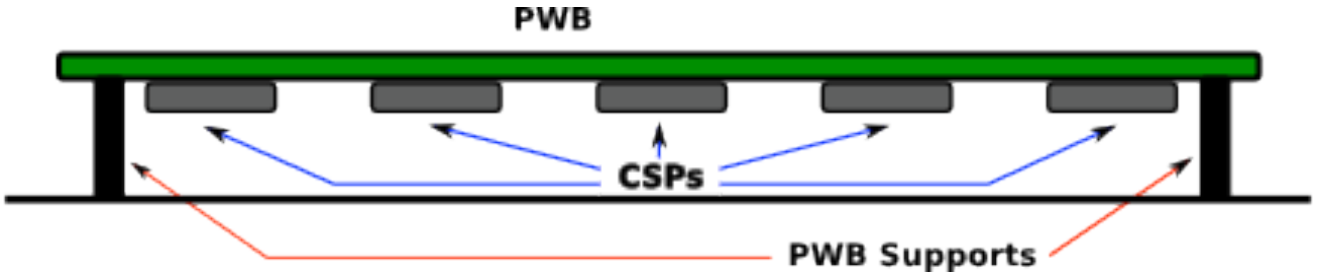


Reliability Test Design

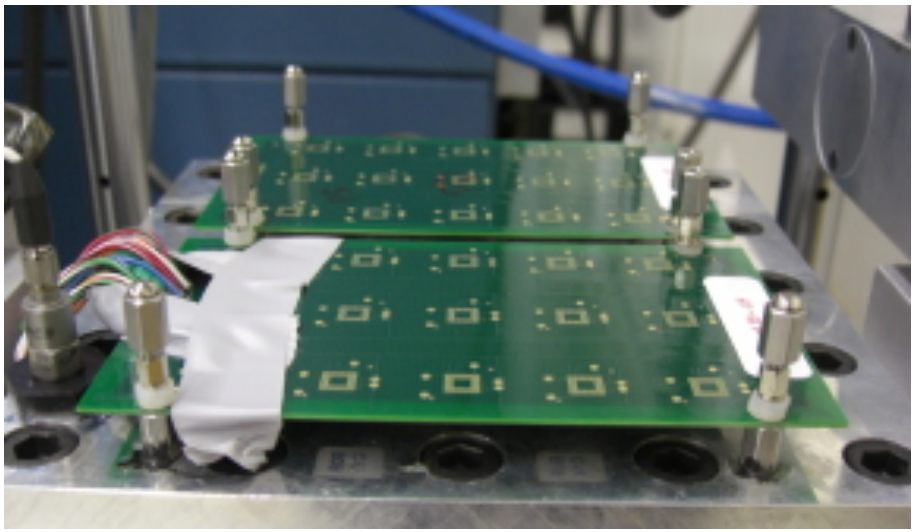
- Two failure detection systems
- Three acceleration conditions
- Edge-bonded and not edge-bonded CSPs

Failure Detection	DAQ System		Post-Drop System	
Edge-bonding	Yes	No	Yes	No
900 G – 0.7 ms	0	3	0	3
1500 G – 0.5 ms	4	3	4	3
2900 G – 0.3 ms	4	1	4	0

Test Vehicle Orientation



The test vehicle is always mounted with the CSPs face down (toward the drop table); this is the worst-case orientation for reliability of the solder joints



Component Locations

- JEDEC defined component numbering
  - Our DAQ cable attaches at component 1–6–11 end
  - As shown components are underneath board

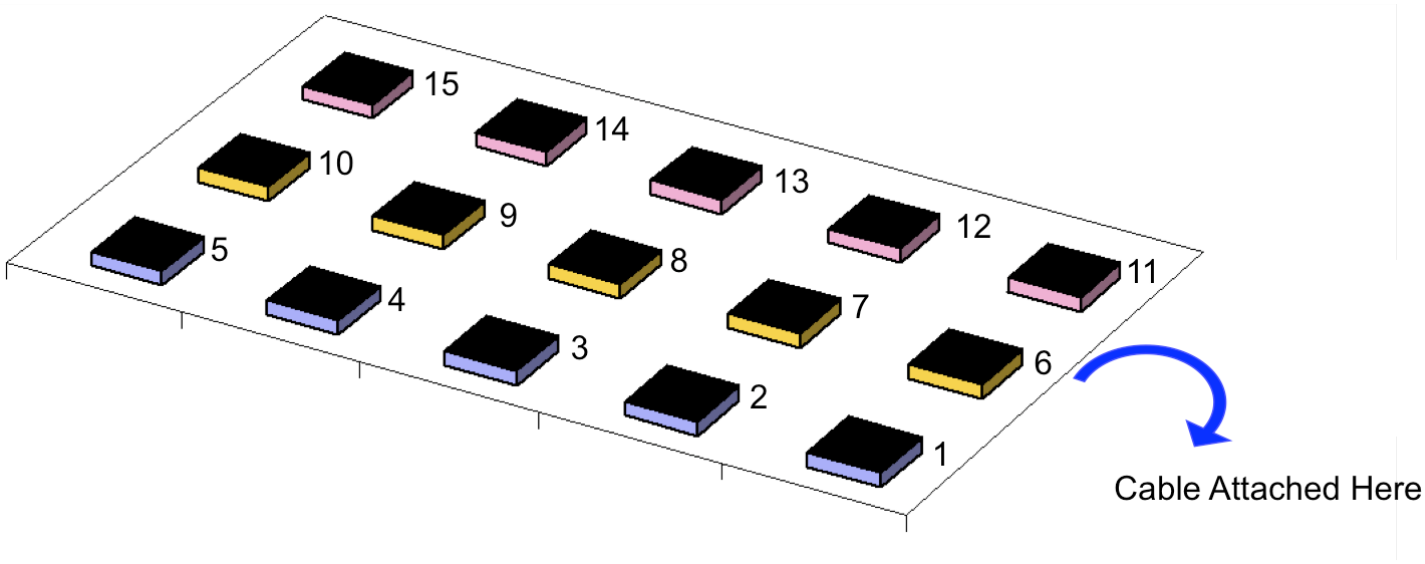


Table 2 - DAQ No Edge-bond

Accel (g)	900	900	900	1500	1500	1500	2900
Drops	75	75	100	70	40	60	50
Edge Bond	None	None	None	None	None	None	None
Component							
C1				**37**	**29**		**7**
C2							**25**
C3	**62**				**14**	**33**	**4**
C4	**26**	**26**	**34**	**26**	**6**	**23**	**4**
C5							**5**
C6					**21**	**35**	**3**
C7					**19**		**42**
C8	**28**	**44**		**50**	**3**	**13**	**7**
C9					**30**		**21**
C10							
C11					**5**		**11**
C12	**16**	**6**	**43**	**13**	**2**	**6**	**4**
C13	**15**	**11**	**40**	**9**	**1**	**5**	**2**
C14					**21**	**32**	**38**
C15							**50**

Table 3 - Post-drop No Edge-bond

Accel (g)	900	900	900	1500	1500	1500
Drops	75	70	100	70	40	60
Edge Bond	None	None	None	None	None	None
Component						
C1			**82**	**55**		**38**
C2						**22**
C3	**7**	**31**	**15**	**8**	**3**	**11**
C4	**10**	**43**	**17**	**7**	**5**	**36**
C5	**65**	**2**	**14**	**1**	**5**	**14**
C6	**54**					**45**
C7			**61**			**9**
C8	**13**	**13**	**16**	**7**	**5**	**2**
C9	**53**	**16**	**11**	**28**	**8**	**14**
C10						
C11	**29**		**55**			**12**
C12	**6**	**9**	**18**	**5**	**3**	**3**
C13	**5**	**28**	**16**	**5**	**3**	**3**
C14	**1**		**37**	**5**	**34**	**4**
C15	**44**		**75**	**26**		

Table 4 - DAQ with Edge-bond

Accel (g)	1500	1500	1500	1500	2900	2900	2900	2900
Drops	325	350	279	355	190	170	175	173
Edge Bond	Heat	Heat	UV	UV	Heat	Heat	UV	UV
Component								
C1						**151**	**66**	**61**
C2		**342**	**276**		**133**	**127**		**119**
C3	**80**	**292**	**33**	**101**	**70**	**72**	**12**	**103**
C4	**236**	**255**	**257**		**63**	**16**		**100**
C5						**36**	**73**	**91**
C6		**55**				**44**	**37**	**60**
C7						**35**	**69**	**158**
C8	**201**			**85**	**113**	**20**	**84**	**83**
C9				**292**		**25**	**29**	**124**
C10			**277**			**12**	**59**	
C11		**193**	**178**	**103**		**65**	**38**	
C12	**66**	**76**	**52**	**162**	**53**	**24**	**23**	**16**
C13	**61**	**129**	**73**	**77**	**42**	**13**	**18**	**14**
C14		**232**				**42**	**44**	**120**
C15	**107**		**268**		**44**	**22**	**25**	**90**

Table 5 - Post-drop with Edge-bond

Accel (g)	1500	1500	1500	1500	2900	2900	2900	2900
Drops	237	350	279	300	170	170	175	173
Edge Bond	Heat	Heat	UV	UV	Heat	Heat	UV	UV
Component								
C1		**304**	**62**			**12**	**23**	
C2			**101**				**34**	**98**
C3	**2**		**180**	**81**	**74**	**72**		**23**
C4	**2**	**292**	**99**	**242**		**25**	**13**	
C5	**60**		**62**	**262**		**40**		**151**
C6	**112**	**282**	**180**			**151**		
C7		**6**						
C8	**88**			**108**		**68**	**30**	**21**
C9		**132**		**283**	**116**	**106**	**53**	
C10		**112**						
C11	**3**	**292**				**112**		
C12	**1**	**36**	**188**	**162**	**137**	**57**	**154**	**128**
C13	**159**	**99**	**188**	**133**	**6**	**144**	**36**	**43**
C14	**60**			**243**			**151**	
C15				**297**				

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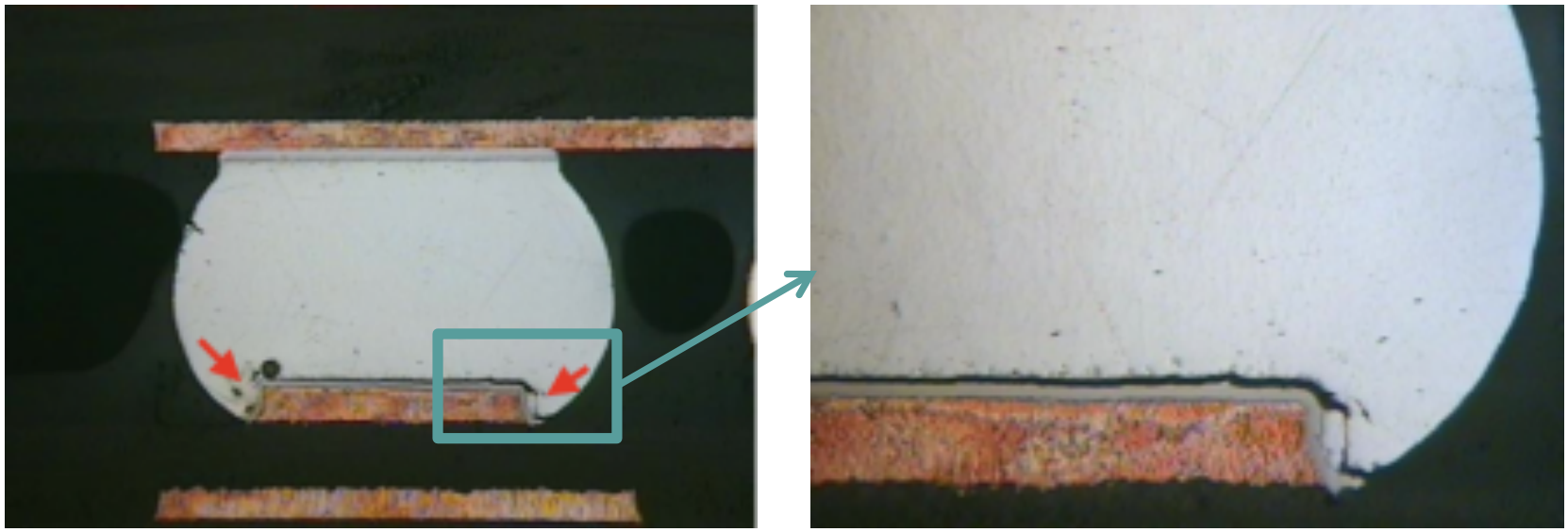
Failure Analysis Methods

- Cross-sectioning with optical or Scanning Electron Microscopy (SEM) imaging
  - Cut open the solder joint, polish the surface, then look for cracks in the solder joint
- Dye Penetrant Method with optical imaging
  - Use red dye to stain cracked solder joints by soaking the test vehicle in dye in vacuum chamber
  - Remove components from the test vehicle, look for cracked/stained failures

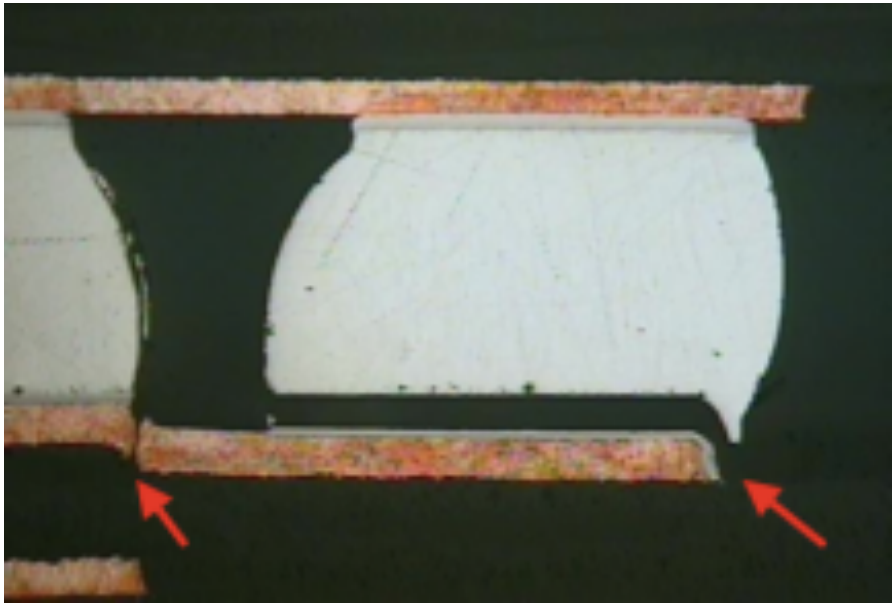
Solder Fracture Failure

- Cross-sectioned solder joint is shown to be cracked near the board side copper pad



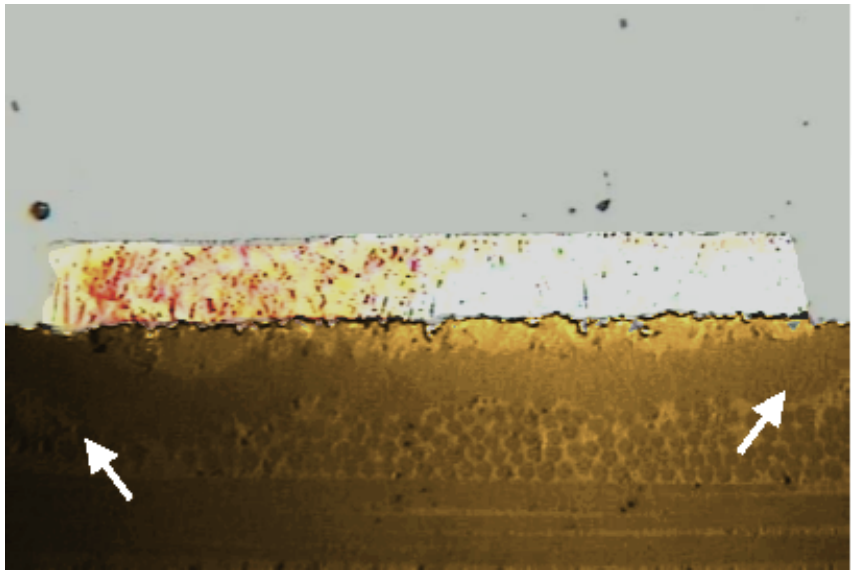
Solder Fracture Failure

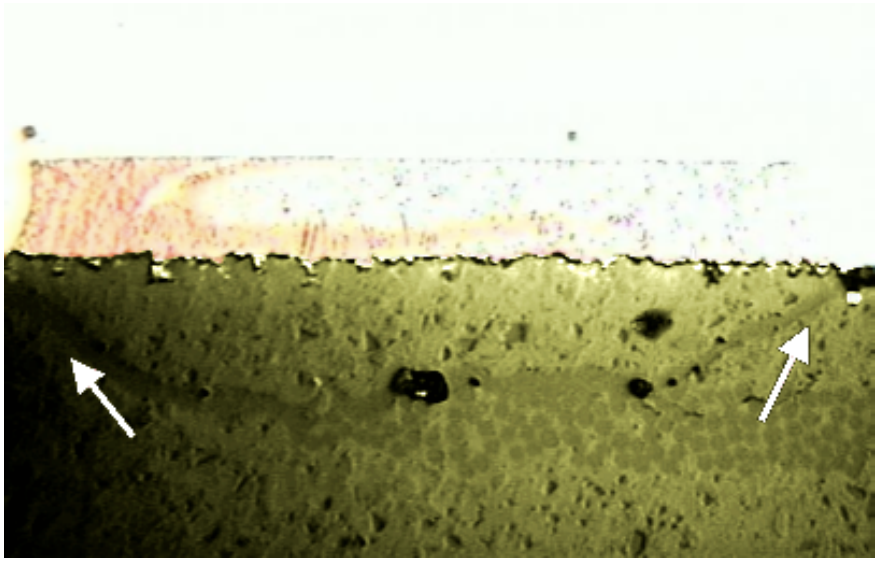
- Cross-sectioned solder joint is shown to be cracked near the board side copper pad
- Copper trace failure also shown (left side)



Cracking Under Pads (Cratering)

- Epoxy on the PWB board surface cracked away from the fibers within the board, allowing the copper pad to lift away from the board





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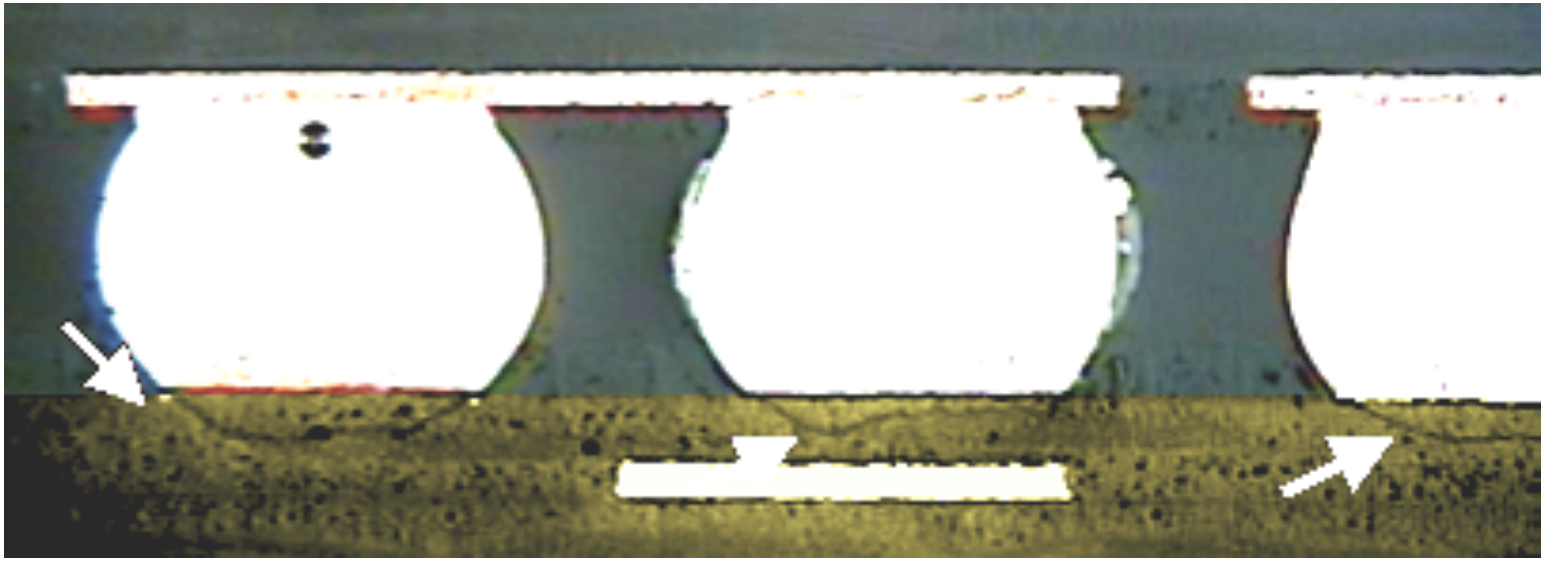
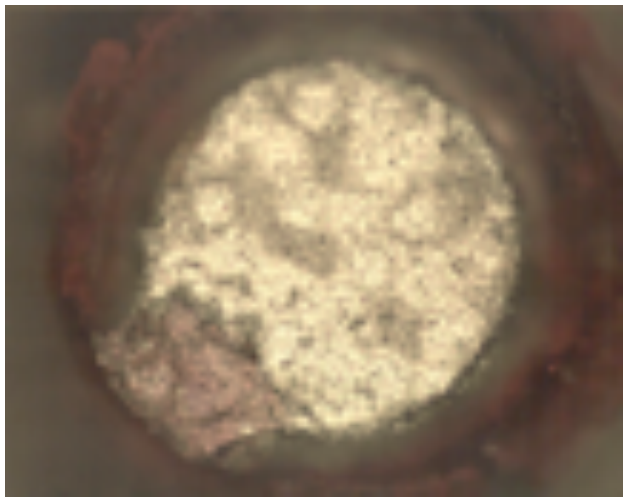


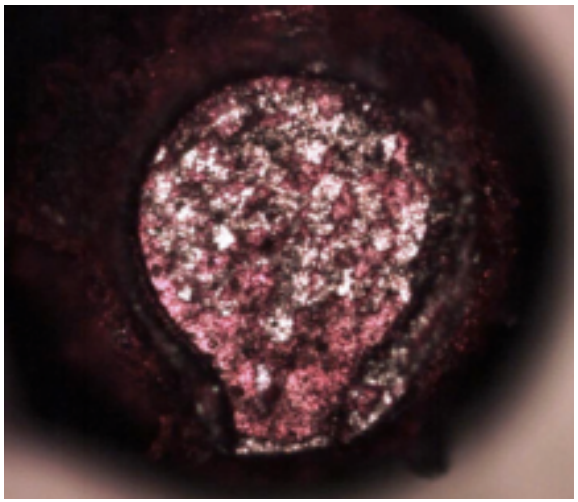
Cracking Under Pads (Cratering)

- Dye penetrant testing was used to determine the extent of pad cratering problems
- Six boards were soaked in dye, then all 15 components were pulled off the boards
- Dye stained solder cracks and pad craters were present before the components were pulled off

Dye Stained Solder Fractures

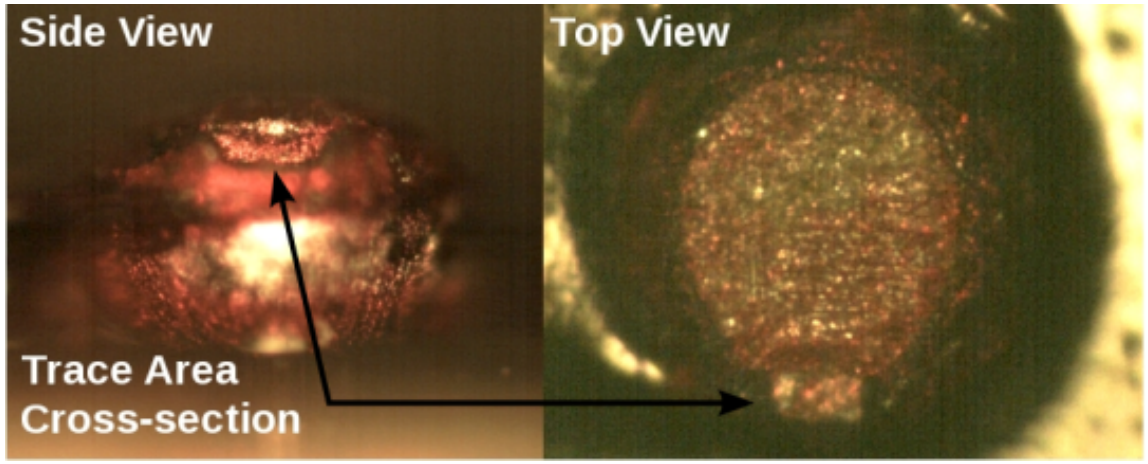
- Dye stained solder cracks were found
  - Partial solder fracture (left) was not completely fractured before the component was removed
  - Complete solder fracture (right) was fully fractured before the component was removed



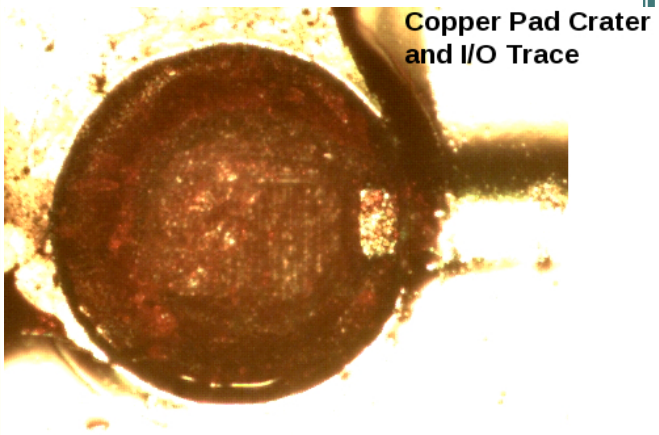


I/O Trace Failure

- Input/Output (I/O) traces that connect to the daisy-chain ‘resistor’ were often broken
- Many components had this broken trace and no other identifiable failure



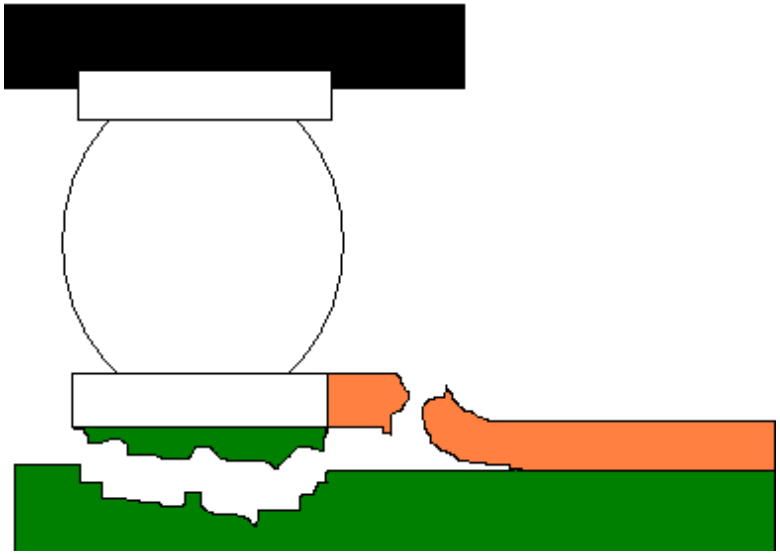
Component side



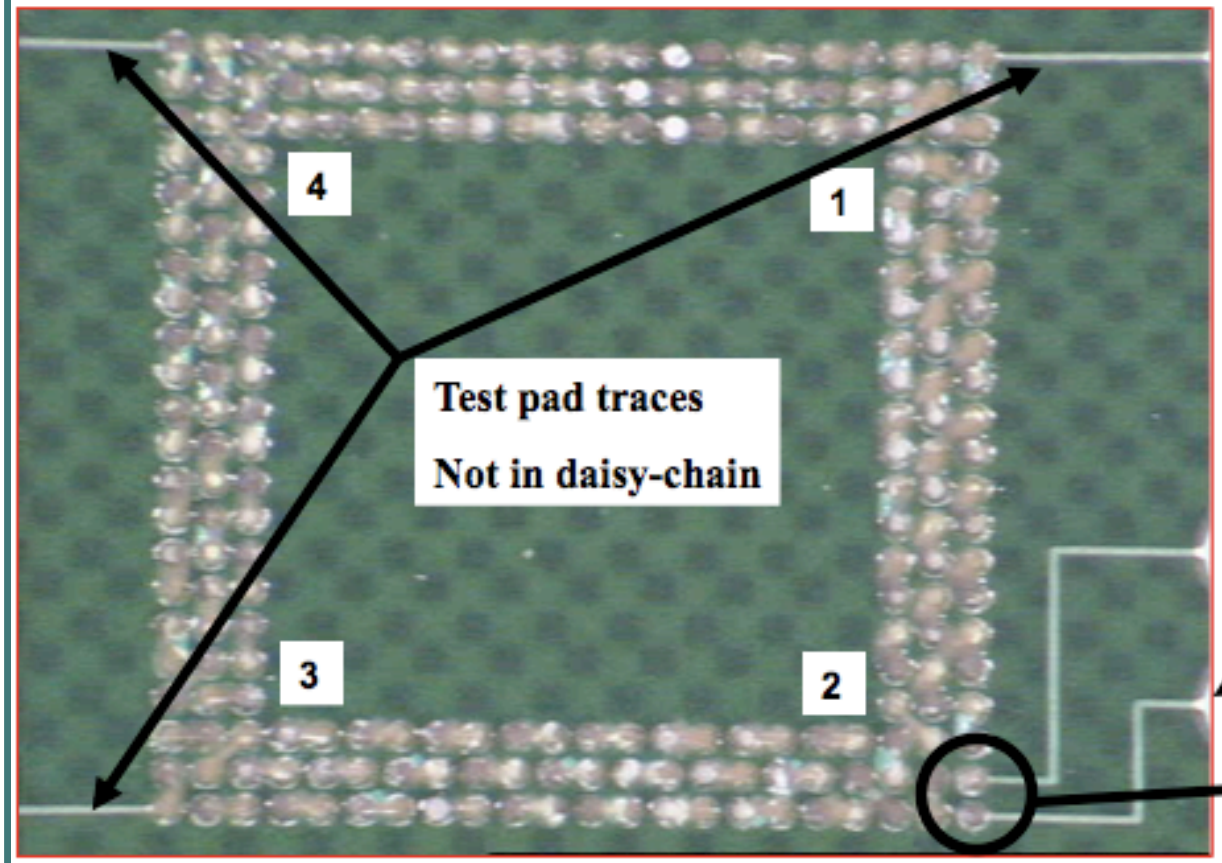
Board side

Illustration of I/O Trace Failure

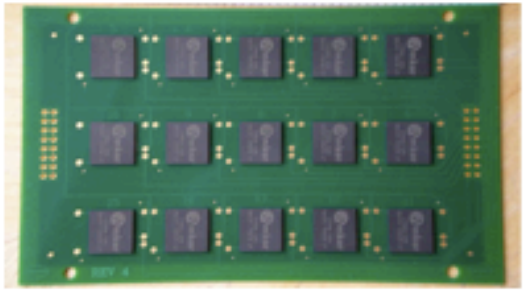
- I/O trace gets stretched when the copper pad lifts away from the PWB
- If the copper pad lifts far enough away, then ductile failure occurs in the copper trace



I/O Trace Failure Location



Solder pad layout for the CSP used in the test vehicle, orientation as board below

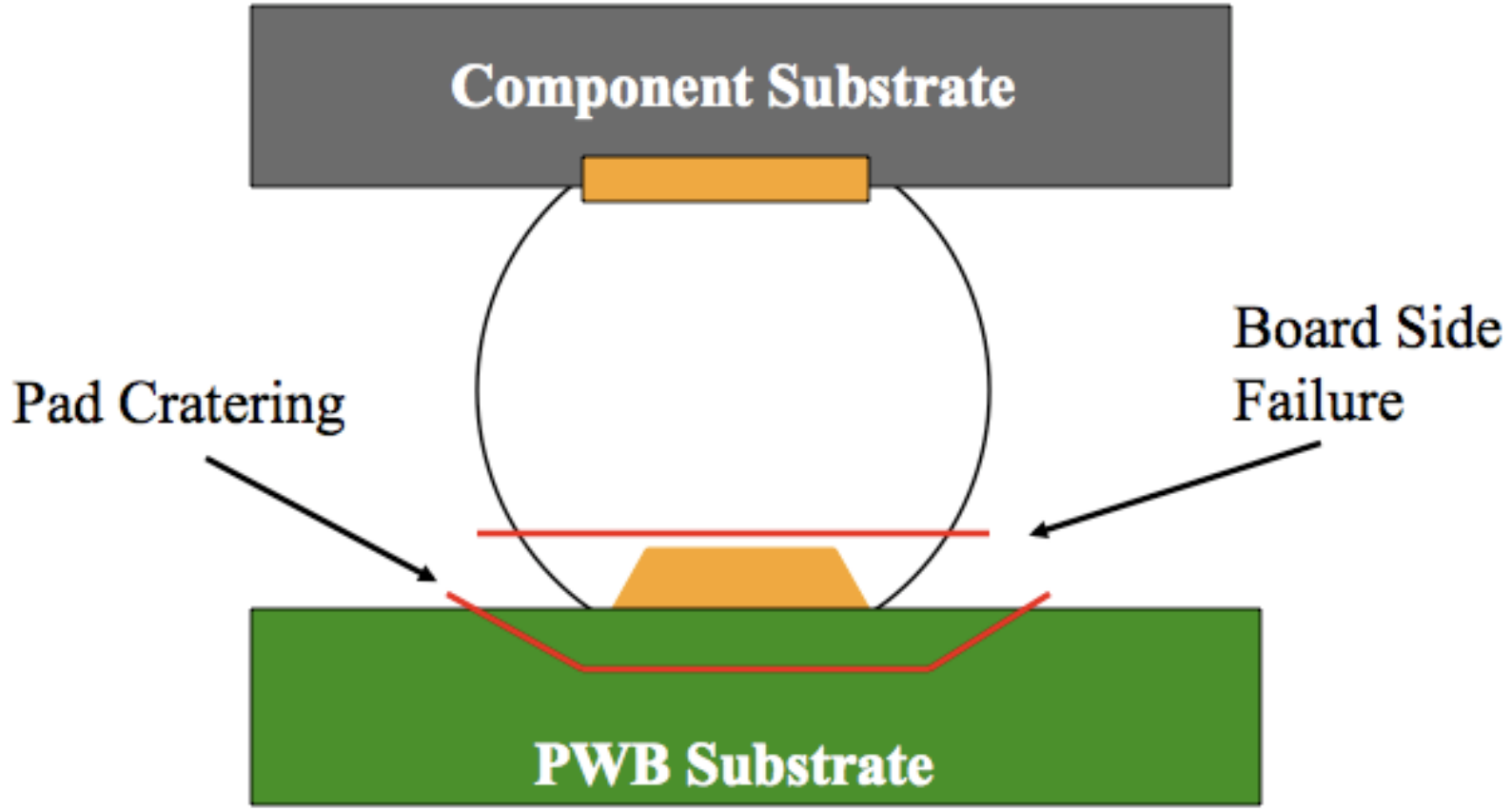


Cable located to the right

Critical Signal Traces

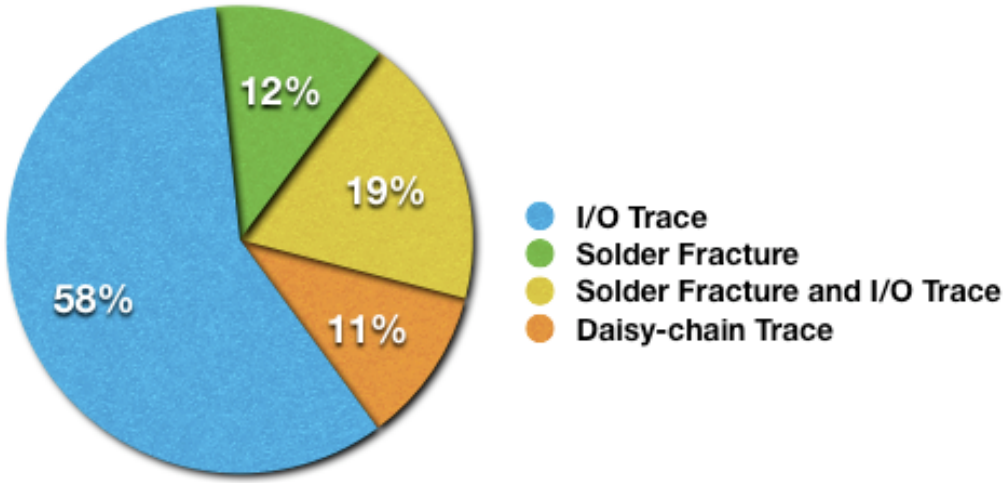
Area where I/O failure occurs most often

Illustration of Failure Locations

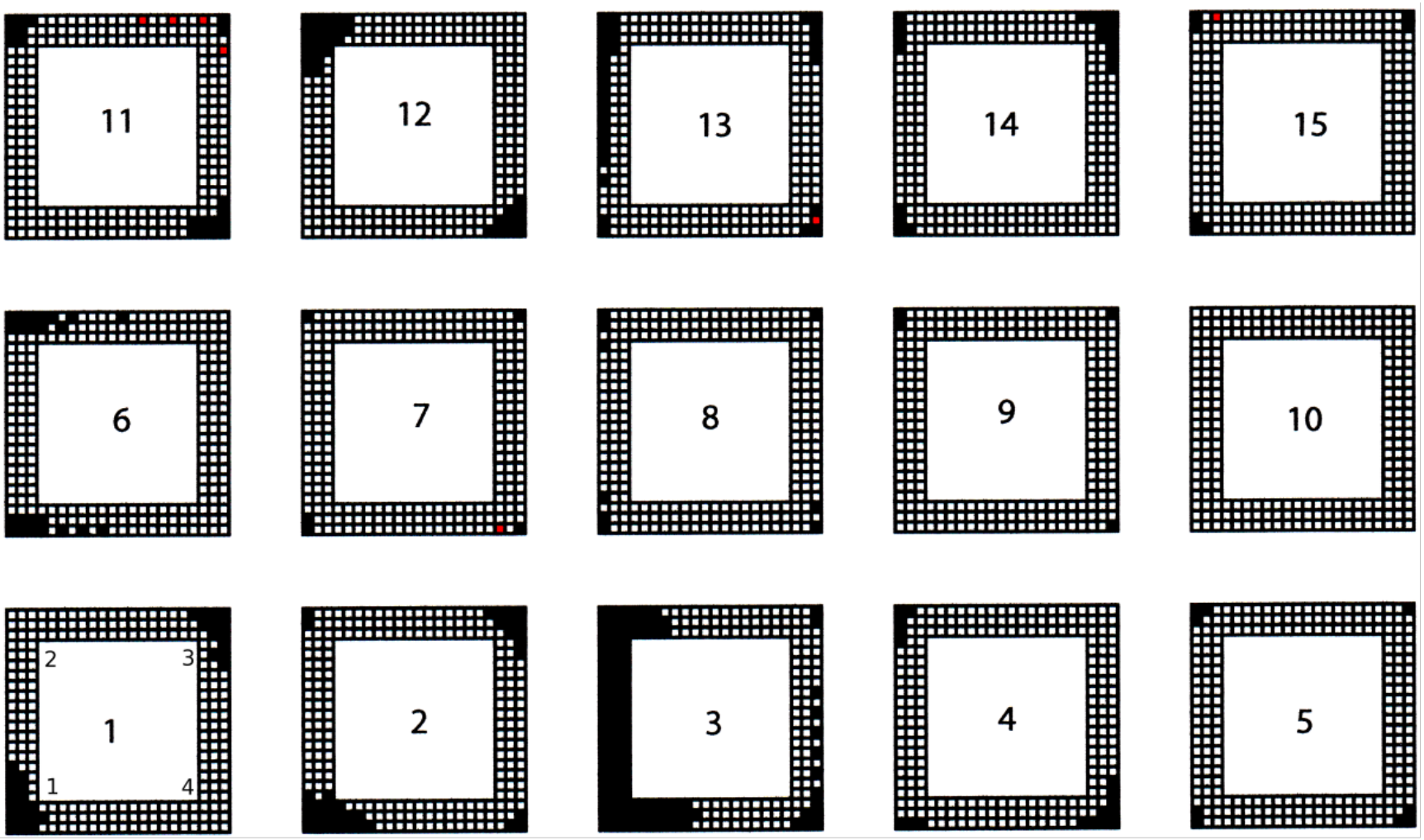


Failure Mode Comparison

- I/O Trace and Daisy-chain Trace failures are both caused by pad cratering
- Pad cratering occurred on 88% of electrically failed components, and is directly responsible for 69% of all electrical failures



failmap-b41-noeb-10drops



Agenda

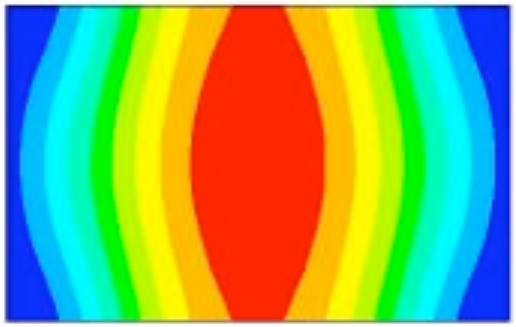
- Drop Impact Testing
- Analysis
  - Reliability Data
  - Failure Mechanisms
  - Acceleration on Test Vehicle
- Conclusions
- Acknowledgements

Cable Influence on PWB Loading

- Results from the comparison of failure detection methods
  - The DAQ system cable attached to the PWB appears to effects loading conditions
  - Fewer components fell off the DAQ tested boards than off the post-drop tested boards
  - The earliest component failure locations vary between DAQ and post-drop tested boards

PWB Loading Conditions

- JEDEC drop testing causes a complex PWB strain condition; not all solder joints experience the same stress and strain
  - Reliability and failure analysis must consider component location, drop count, and acceleration pulse profile



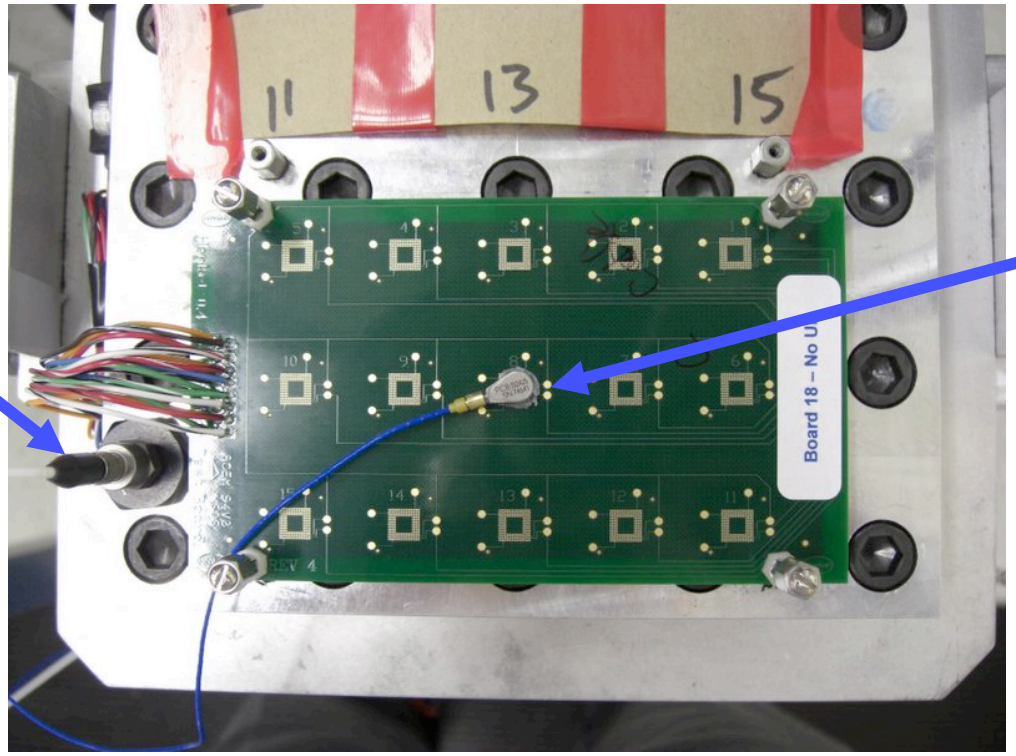
(Strain distribution image from JEDEC JESD22-B111)

Local Acceleration Conditions

- Using two accelerometers, the acceleration profile of the board at each component location was tested
- Eight board variations
  - Blank PWB, Populated, with edge bond, and without edge bond
  - With and without DAQ cable soldered into the board

Local Acceleration Conditions

Accelerometer on Drop Table



Accelerometer above Component 8

Testing the acceleration condition on the board and table simultaneously

Local Acceleration Conditions

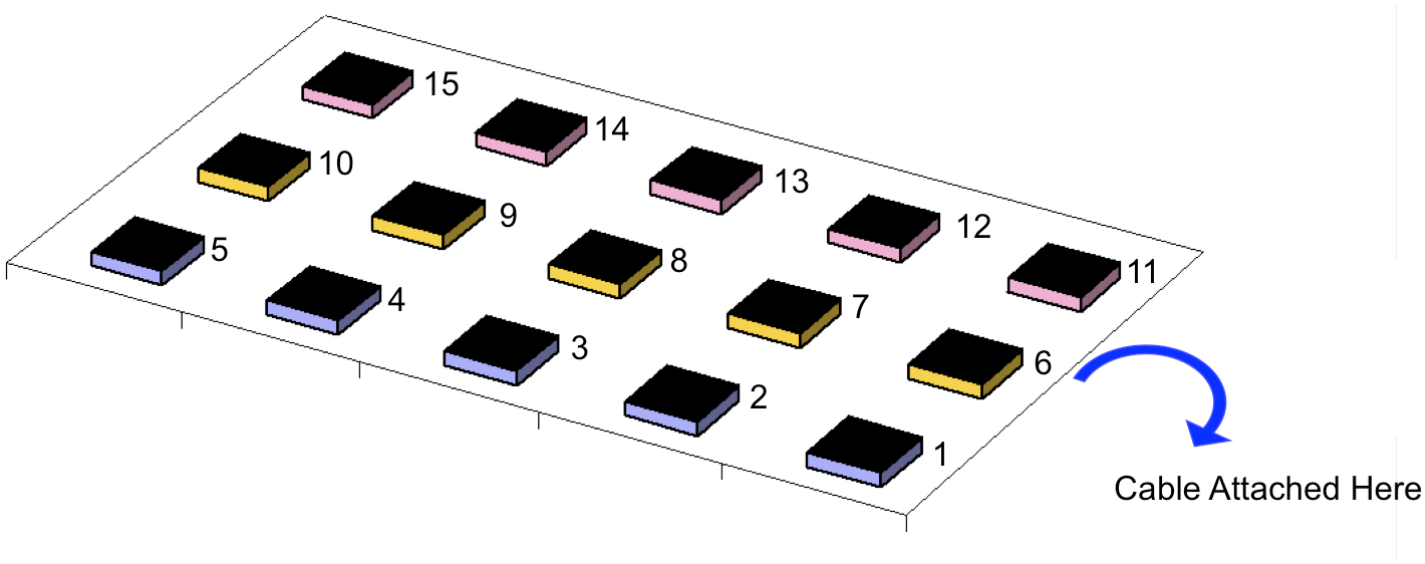
- Table baseplate has insignificant vibration
- Board vibrates over period longer than 10ms

Acceleration vs Time

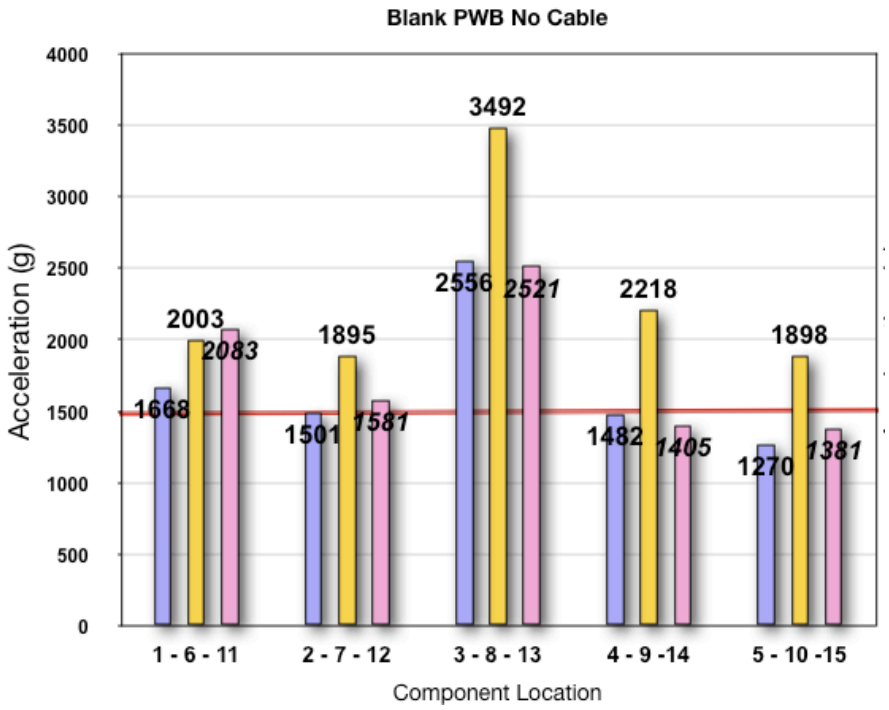
	Channel Description:	G's	msec	In/S	Filter Hz	Max G's	Min G's
Ch1	Channel 1	1538.81	0.48	157.25	5000.00	1538.81	-44.09
Ch2	Channel 2	3834.61	0.20	185.80	5000.00	3834.61	-2172.47

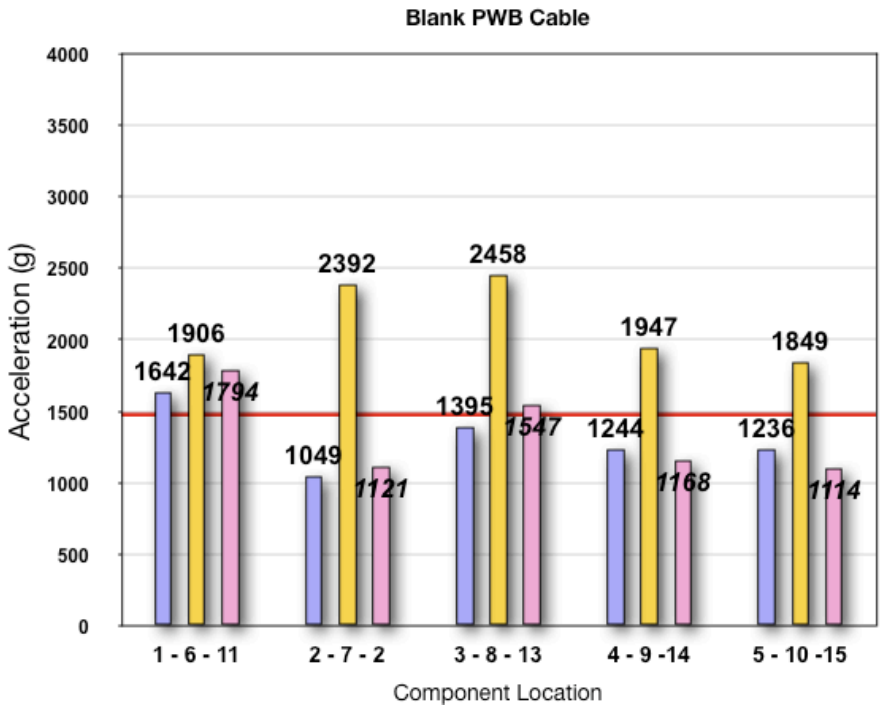
Component Locations

- JEDEC defined component numbering
  - Our DAQ cable attaches at component 1–6–11 end
  - As shown components are underneath board



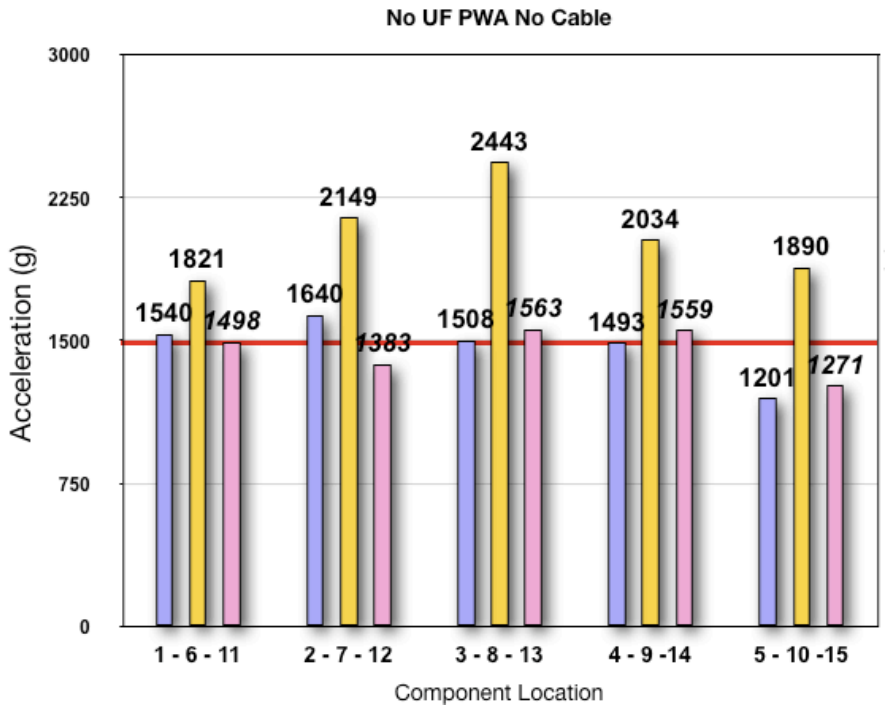
Blank PWB – No Cable vs Cable

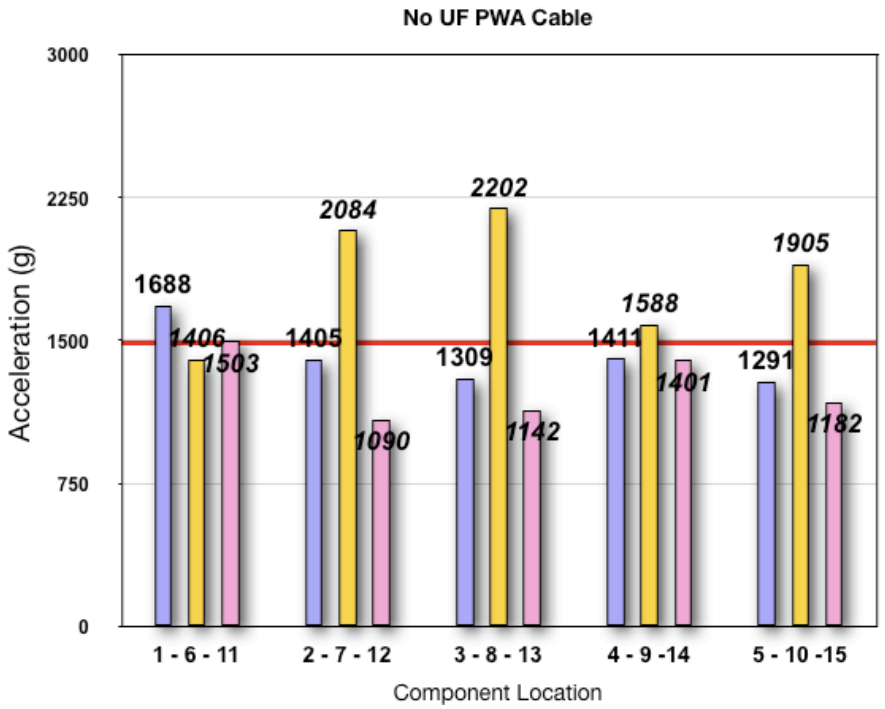




- Apparent differences…
  - Symmetry of acceleration peaks shifted (C7 vs C9)
  - Maximums greatly reduced by cable (C3, C13, C8)

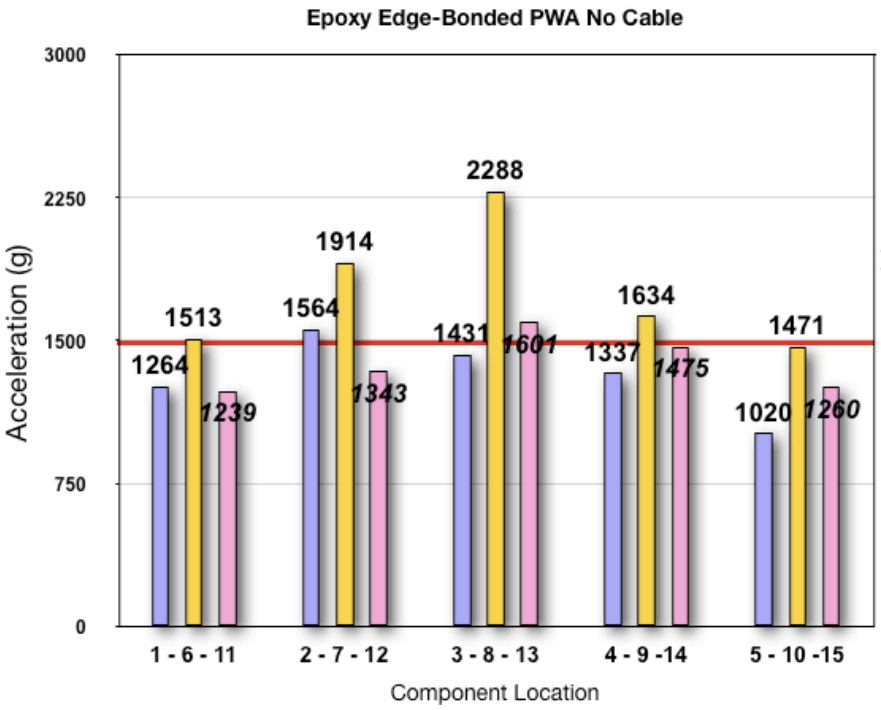
Populated PWB – No Edge Bond

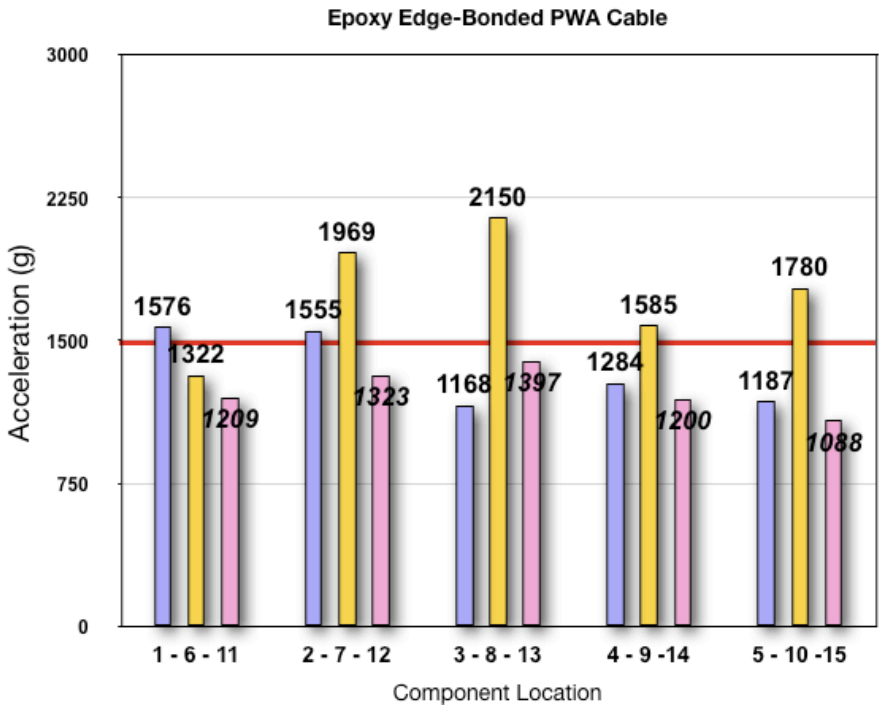




- Dampening due to the cable seems less significant than with blank PWB (both graphs are more similar)

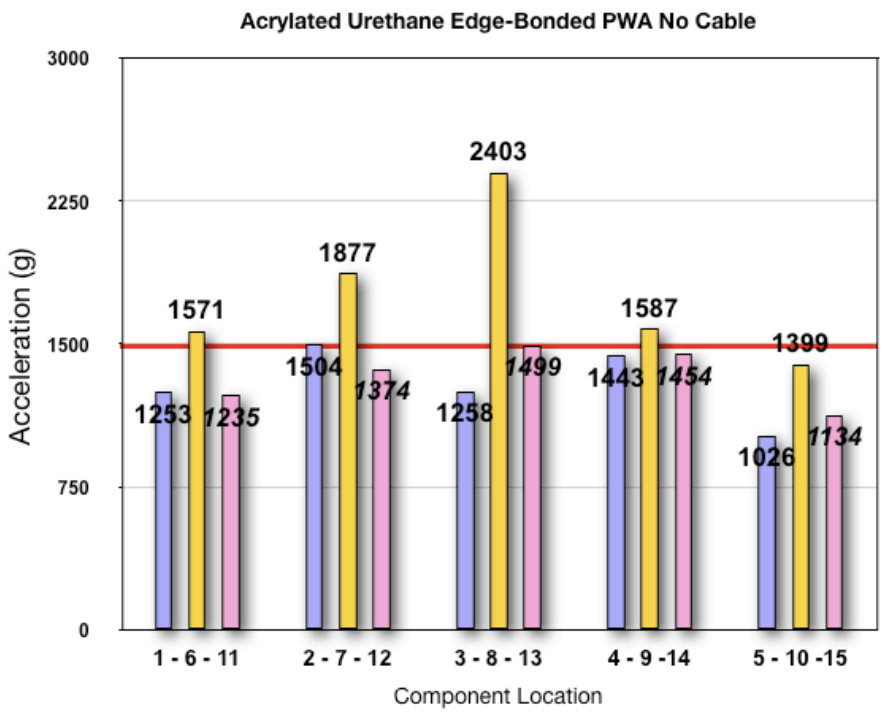
Epoxy Edge Bonded CSPs

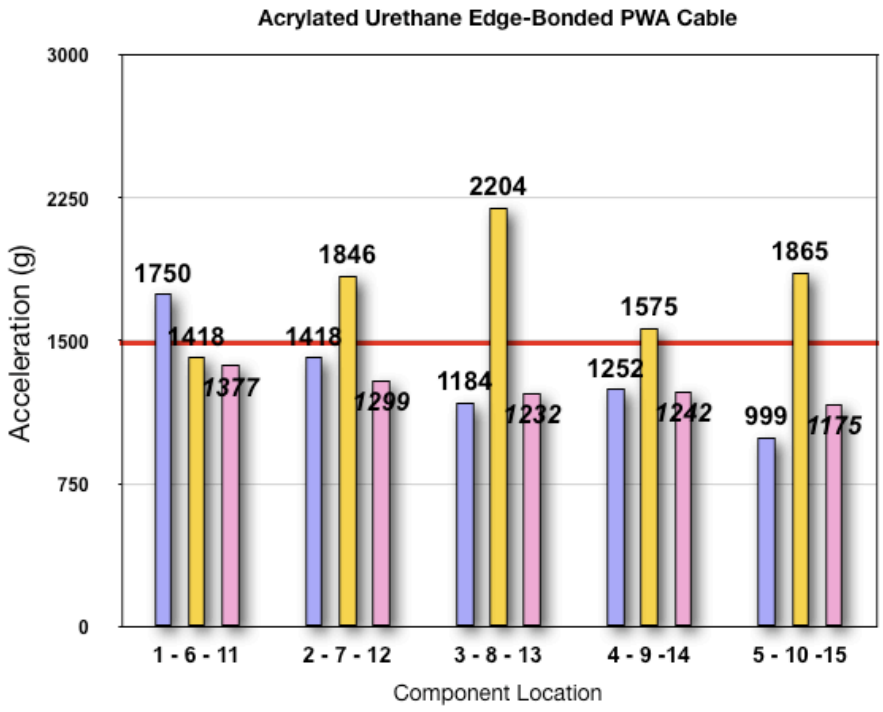




- Stiffer board with edge bonding has less symmetry disturbance
- Overall accelerations are significantly reduced

Acrylic Edge Bonded CSPs





- Stiffer board with edge bonding has less symmetry disturbance
- Overall accelerations are significantly reduced

Cable Influence on Acceleration

- Symmetry of acceleration/deflection/strain is effected:
  - A cable soldered to the PWB will effect the test conditions for any test vehicle assembly
  - Components cannot be grouped as liberally for reliability statistics if test conditions at their locations are not similar
- Lightest possible wire gauge should be used
  - But must provide reliable through-hole solder joints

Cable Influence on Acceleration

- Attaching a cable to both board ends could restore symmetry, but will also…
  - Add mass to the test vehicle
  - Increase vibration dampening
  - Decrease the effects of harmonic vibration frequencies
  - Decrease total deflection (cantilever effect of the wire mass)

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Conclusions

- The component location on the test vehicle has a significant role in reliability
  - Components near the board center tend to fail first
- Higher acceleration conditions decrease the drops to failure, resulting in lower reliability
- Edge bonding significantly increases the reliability of lead-free CSPs in drop impact conditions

Conclusions

- Cohesive failure between the resin and the board fiberglass leads to pad cratering
- Pad cratering causes trace breakage and is the most common electrical failure mode
- Board laminate materials for this lead-free test vehicle are the weakest link in the assembly, rather than the solder

Acknowledgements

- Dr. John Pan (IME), Dr. Albert Liddicoat (EE), Advisors
- Dr. James Harris (EE), Thesis committee member
- Project Sponsors:

FLEXTRONICS

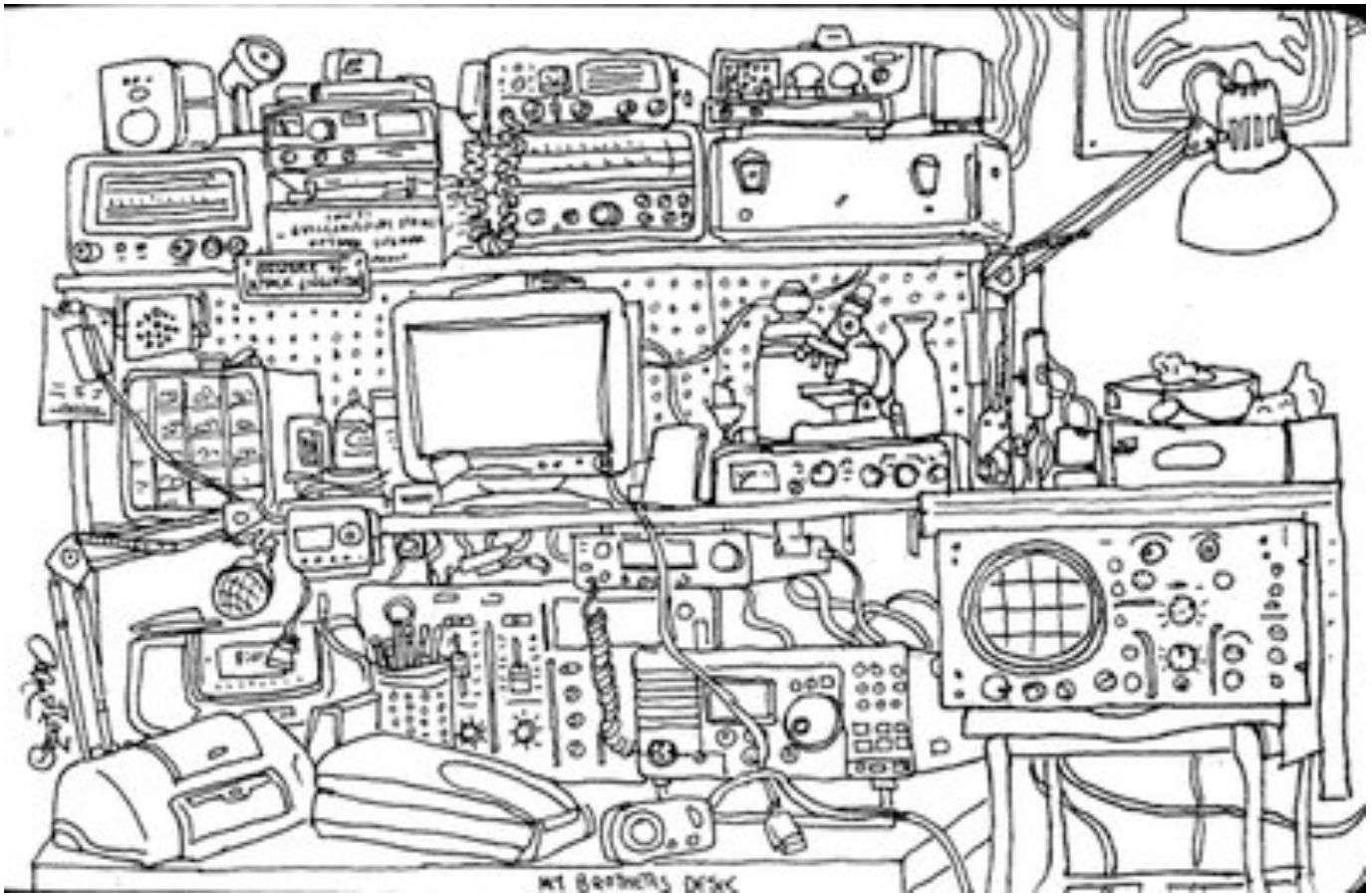
- Office of Naval Research (ONR)

  Through California Central Coast Research Park (C^3RP)
- Society of Manufacturing Engineers Education Foundation
- Surface Mount Technology Association (SMTA)

Acknowledgements

- Multidisciplinary team of students:
  - Nicholas Vickers (MATE), Kyle Rauen (MATE), and Ronald Sloat (ME) assisted with failure analysis
  - Michael Krist (IE) and Micah Denecour (IE) assisted with reliability data analysis
  - Edward Clements (ME) and Chi-Yeh Hsu (ME) built and tested the first data acquisition system prototype
  - Keith Rothman (AERO) wrote the first version of the DAQ system control software

Questions



How do you find an electrical engineer? Look for the 'Desk'.

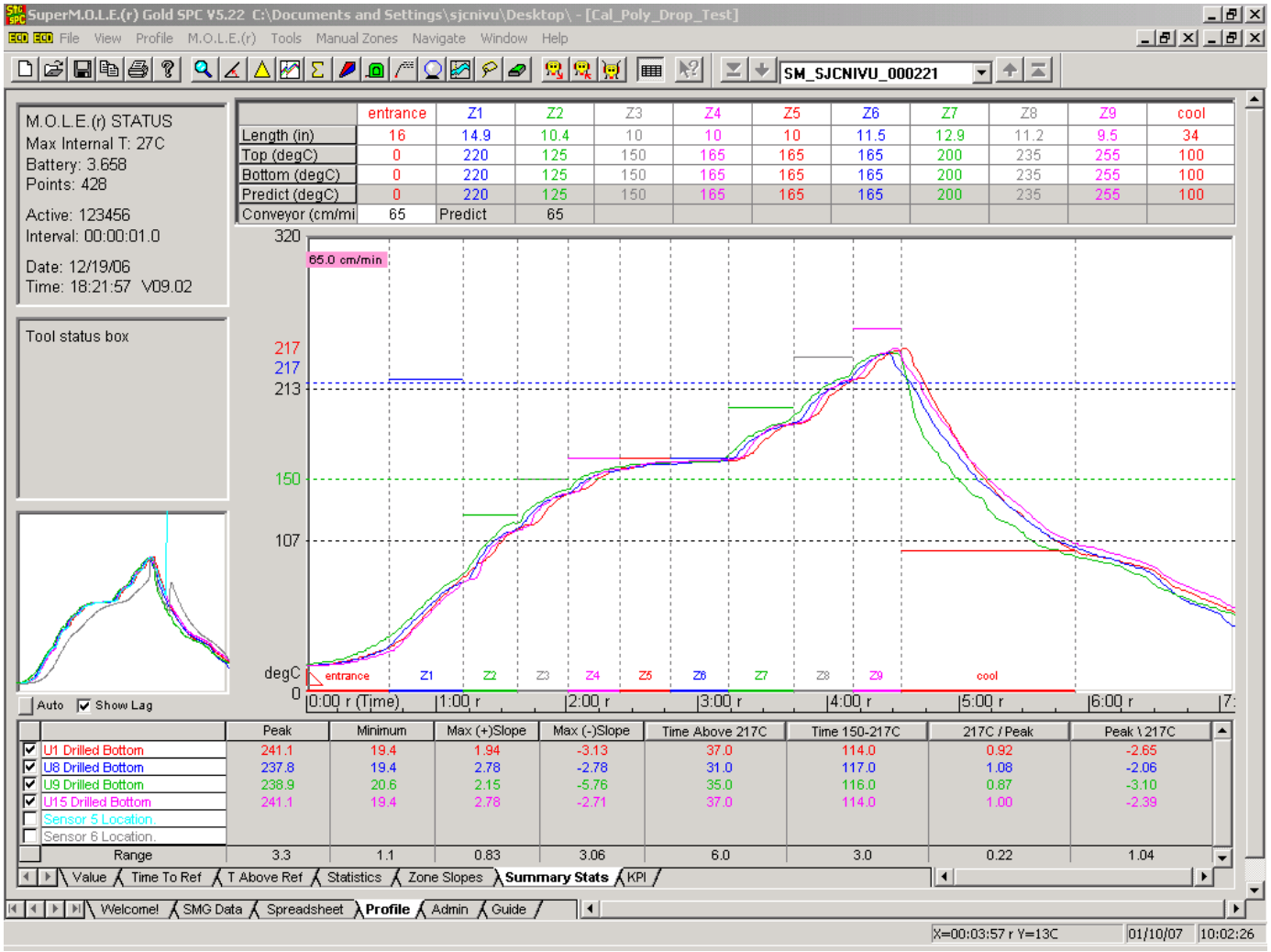
http://comicstripjoint.blogspot.com

Supplemental Slides

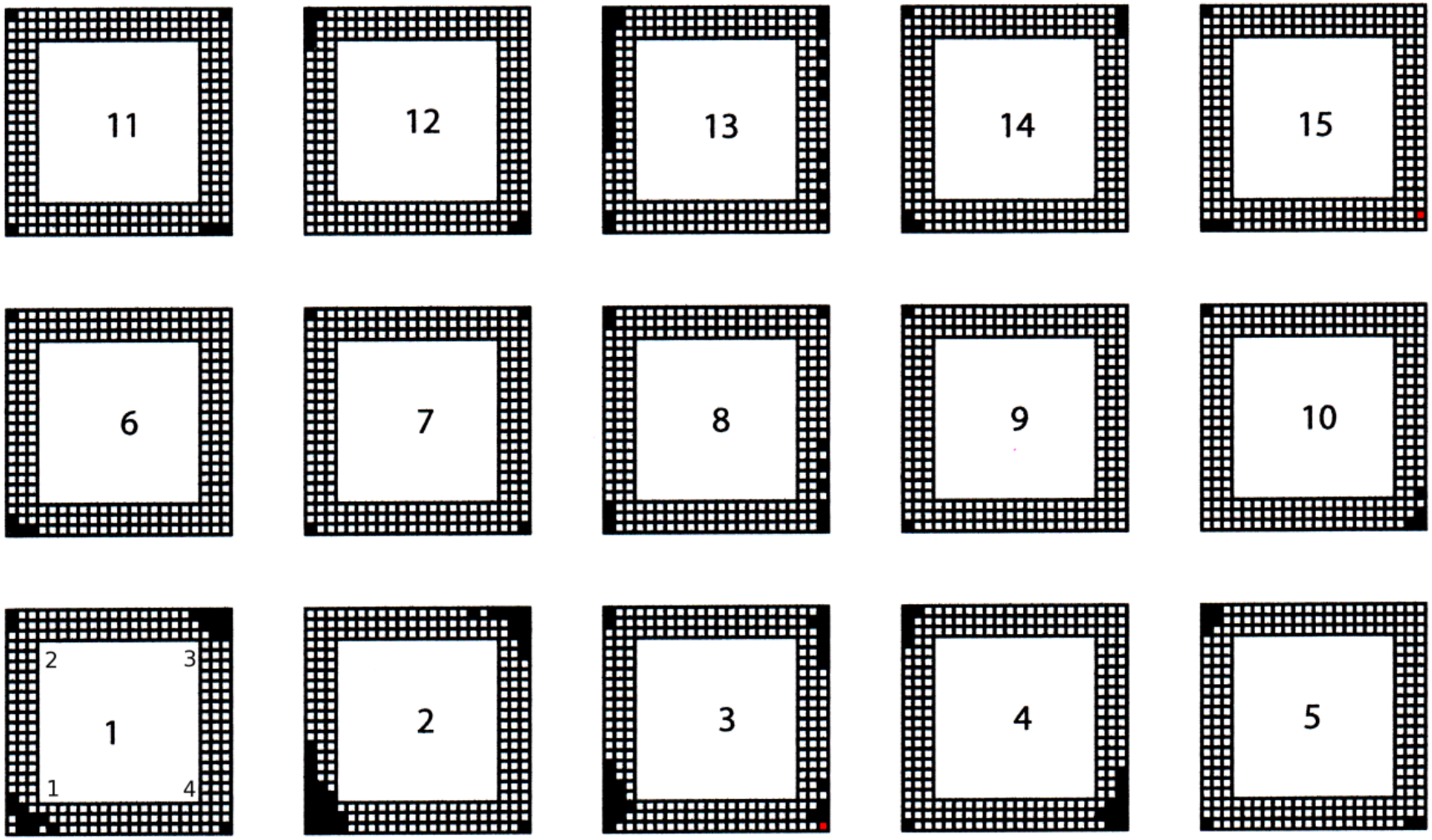
SMT Assembly (stencil printing)

- Stencil (DEK)
  - 4 mils thick
  - Electro-Polish
  - 12 mils square apertures
- Stencil Printing
  - Front/Rear Speed: 40 mm/s
  - Front/Rear Pressure: 12 kg
  - Squeegee length: 300mm
  - Separation Speed: 10 mm/s

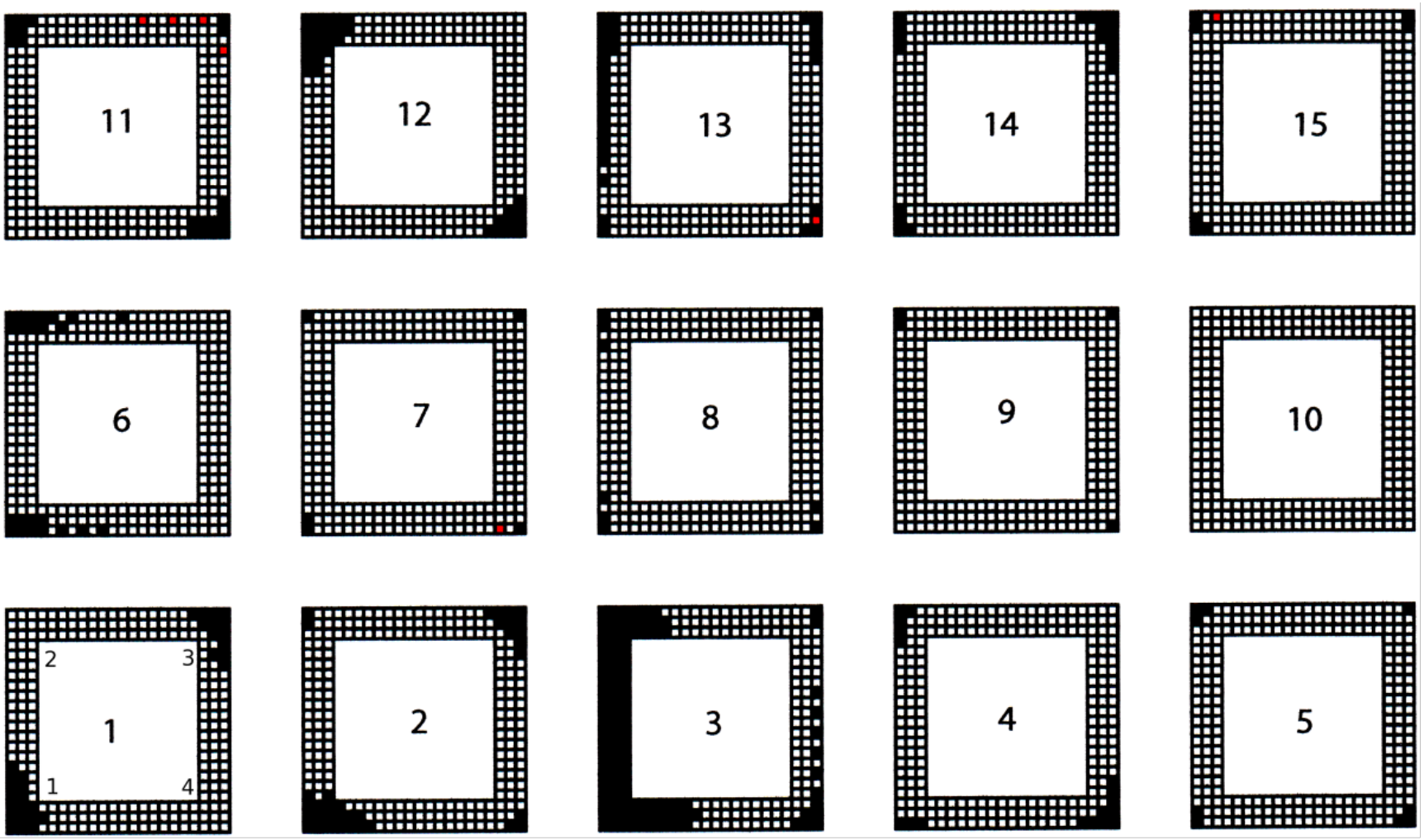
Solder Reflow Profile



failmap-b44-noeb-14drops



failmap-b41-noeb-10drops



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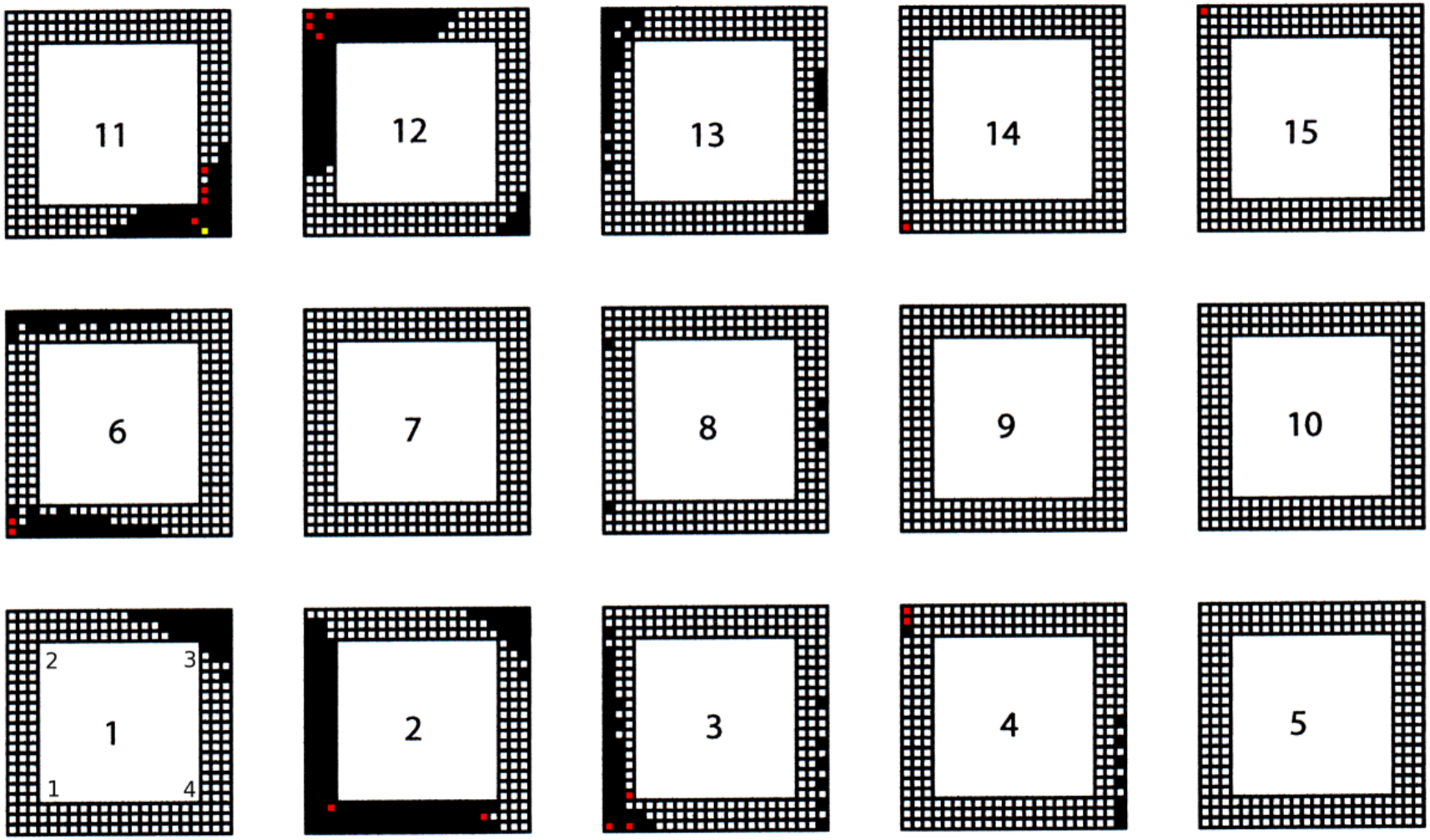

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